SAMIDARE for TPC

C. Santonastaso & the SPADI Alliance

SRO2026

1

The problem

TPC readout at increasing rates

- High-intensity beams require higher-throughput TPC readout.
- Active-target TPCs need many channels and online background rejection.
- GET electronics is becoming obsolete.
- Towards streaming-capable TPC front-end electronics.

2

The SAMIDARE board

What is it

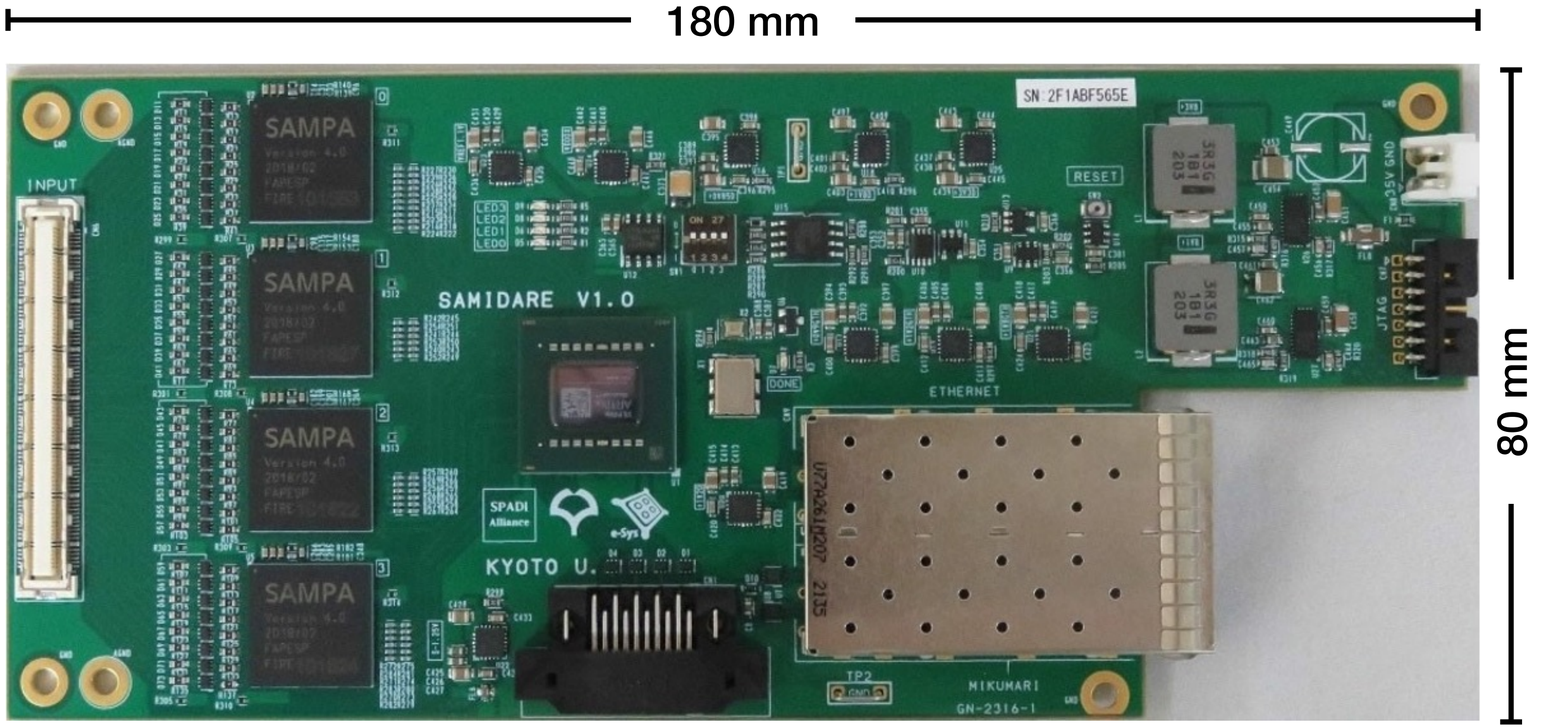
4 x SAMPA chips
(32 Ch, 10 bit @ 10 MHz)

FPGA: Artix UltraScale+

8 ch. GPIO

SFP+ 10GbEthernet

MIKUMARI SFP+[1]

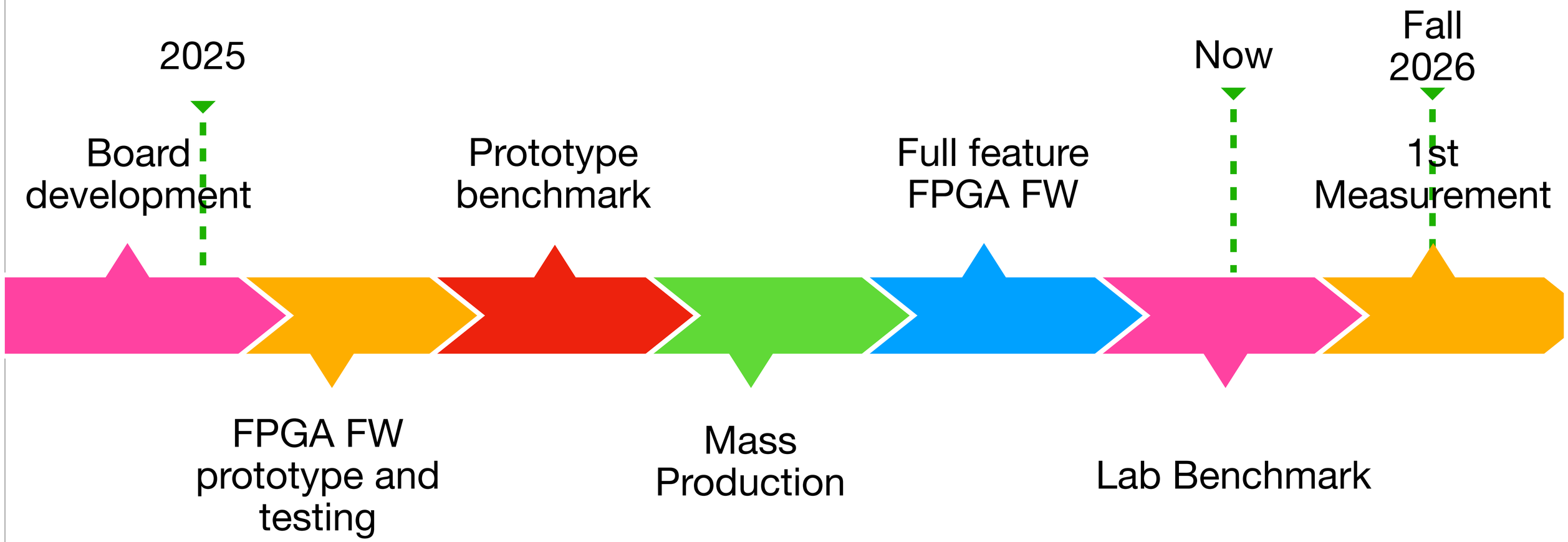


[1] R. Honda - Wednesday @ 14:30

3

Roadmap

SAMIDARE



4

A bit of context

SPADI Alliance

Signal processing and data acquisition infrastructure alliance
toward the standardization for sustainable developments



Main goals:

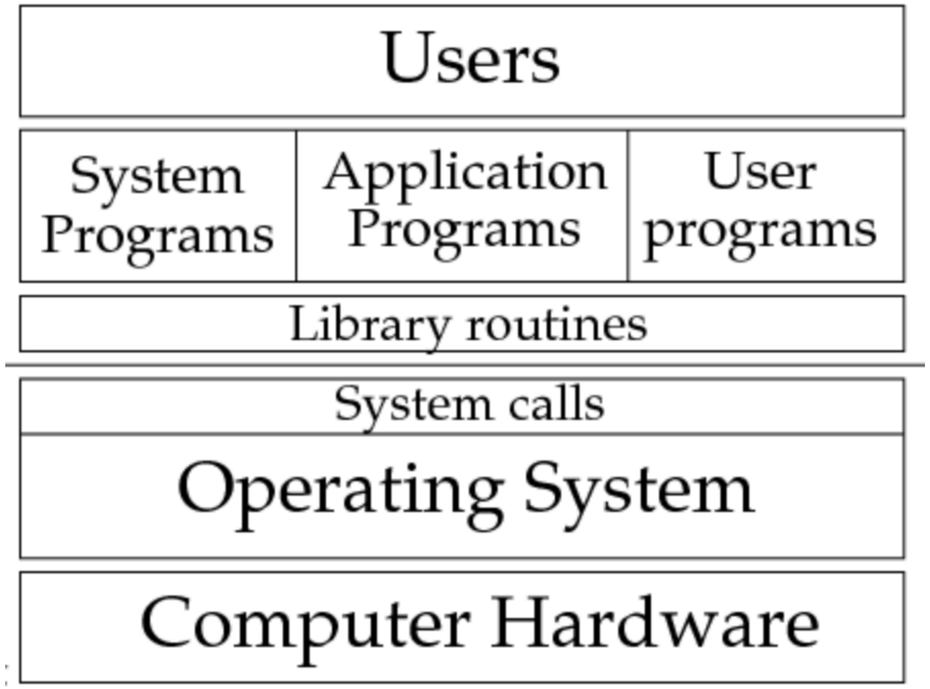
- Common systems
- Standardization
- Reducing costs of development of DAQ systems

5

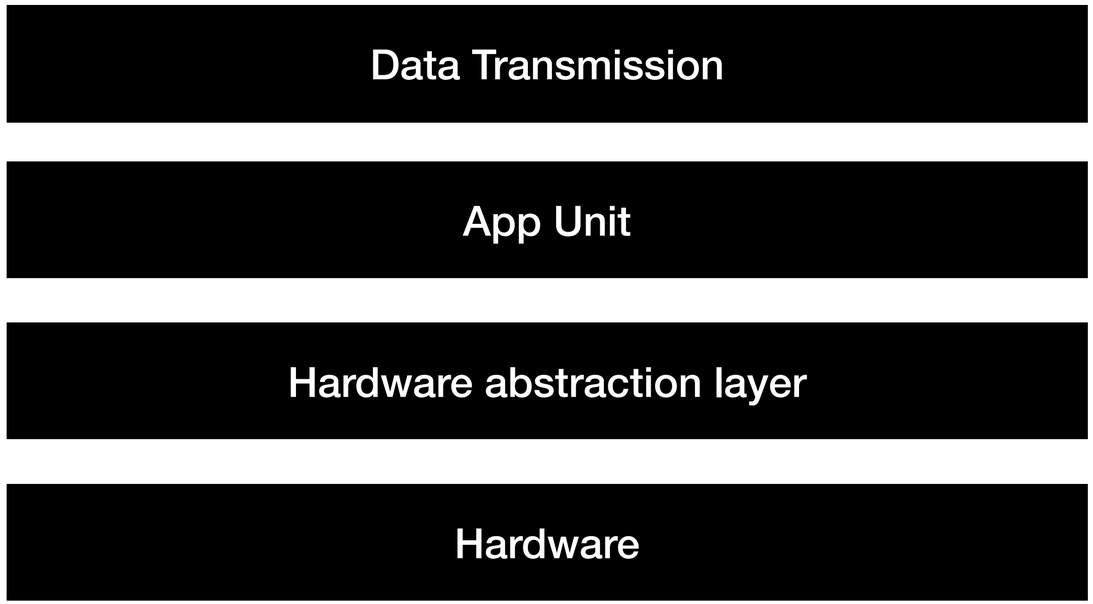
SAMIDARE Firmware

OS-like layering

Software Operating System



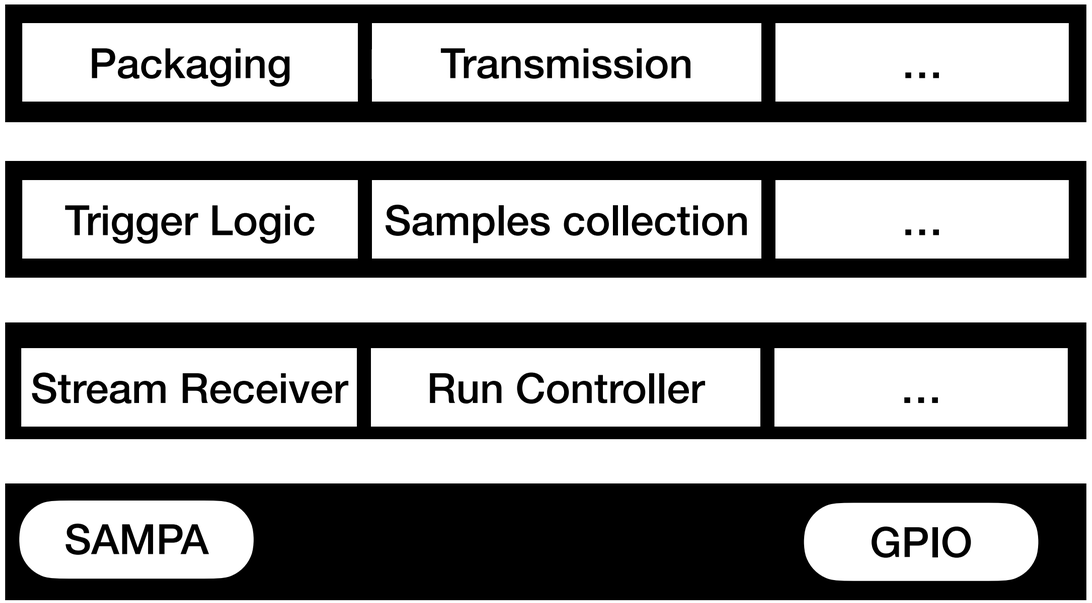
Firmware



6

SAMIDARE Firmware

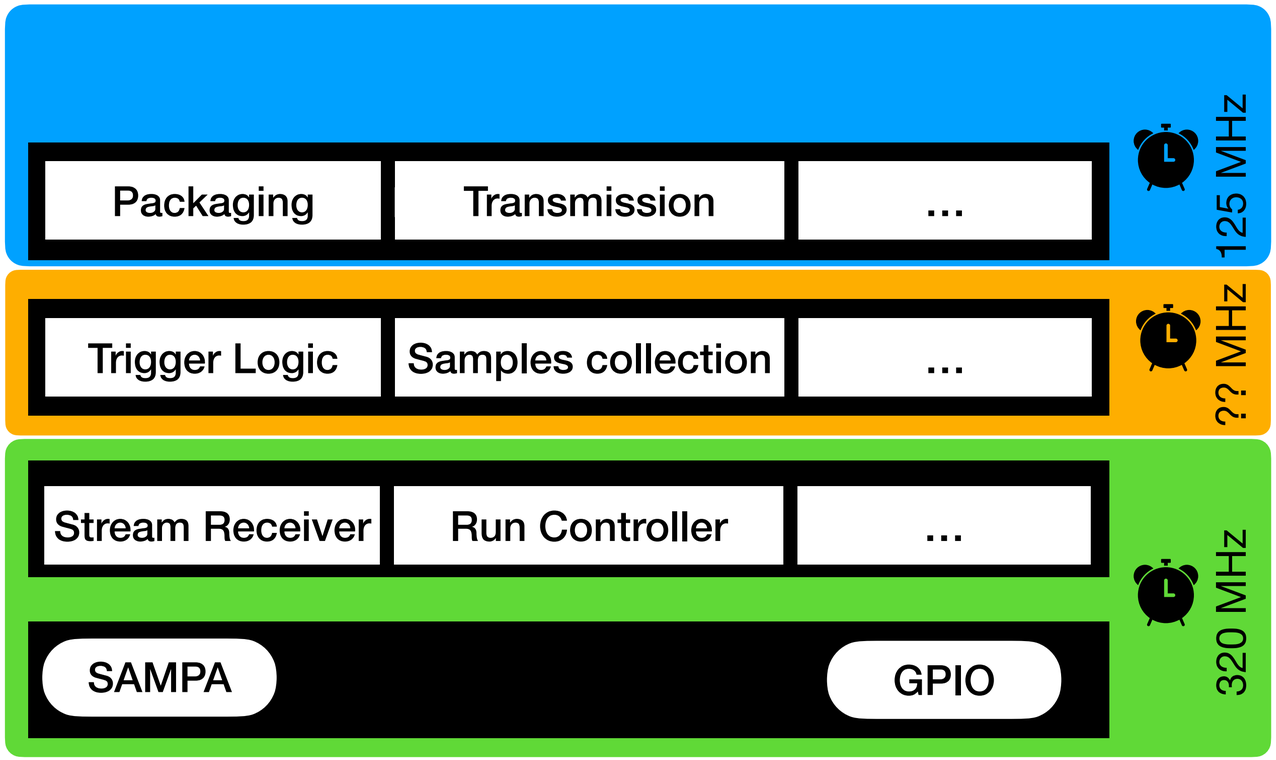
OS-like layering



7

SAMIDARE Firmware

OS-like layering

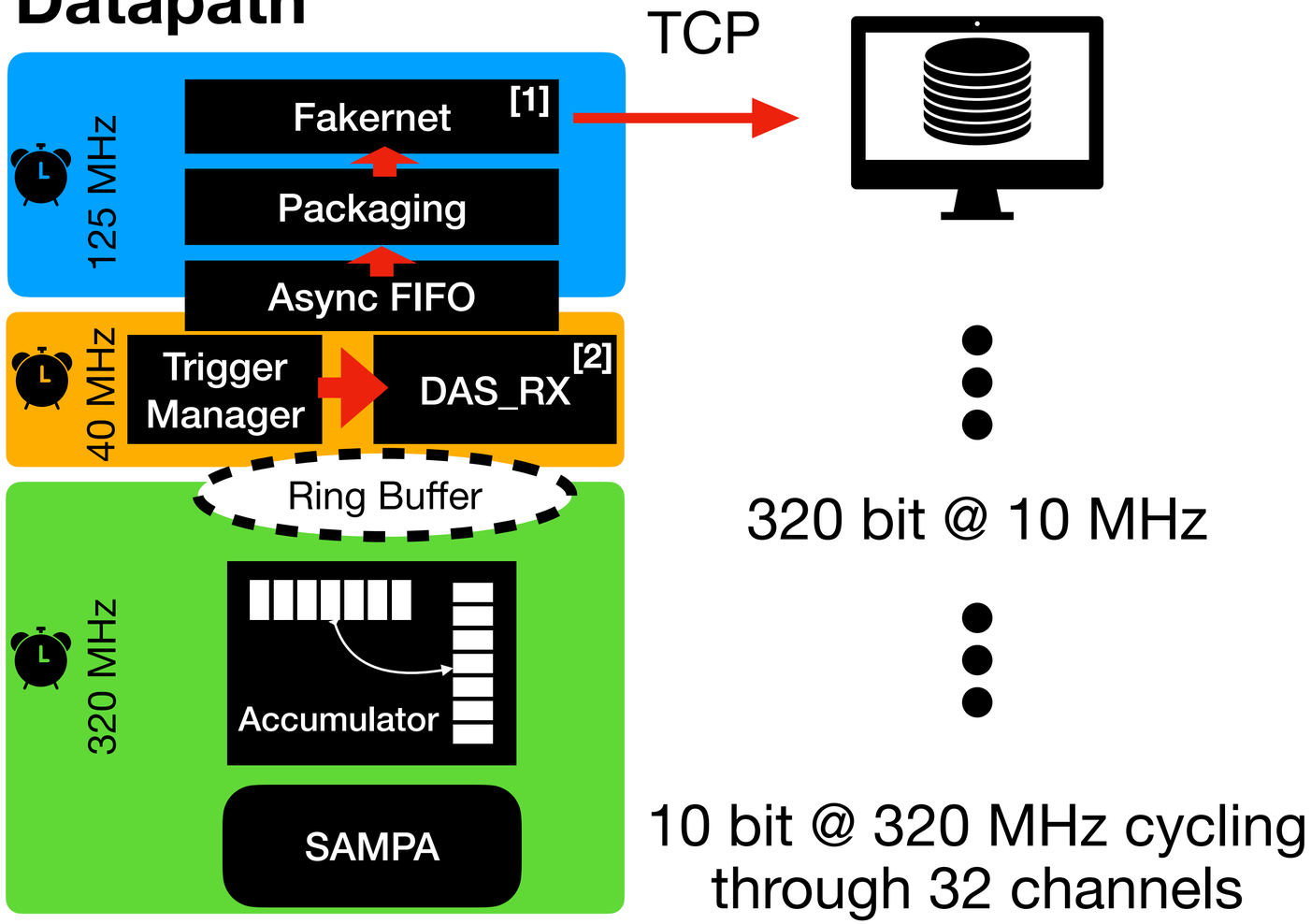


- Facilitate development of specialized firmwares
- Separate application-specific modules from infrastructure modules
- Maintainable and upgradable Firmware

8

Firmware description

Datapath

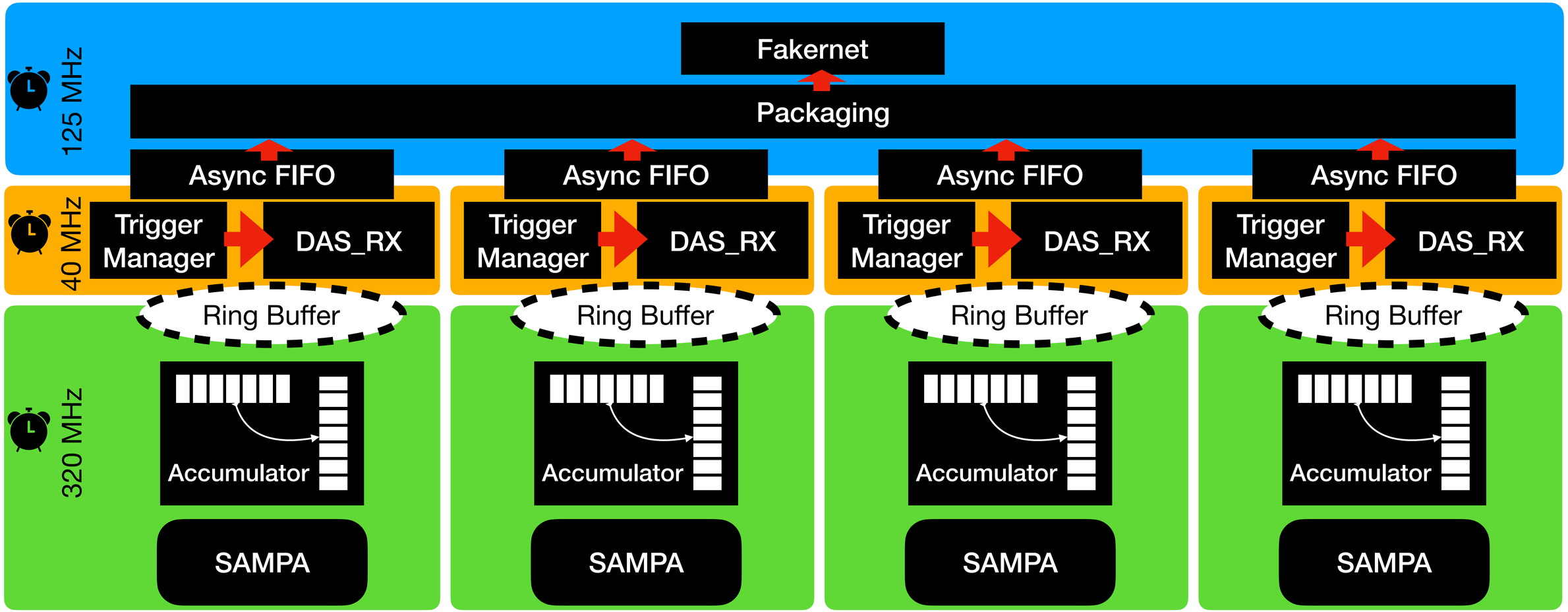


[1] H. T. Johansson, A. Furufors and P. Klenze, Fakernet (2020)
[2] DAS = Direct ADC Serialization

9

Firmware Description

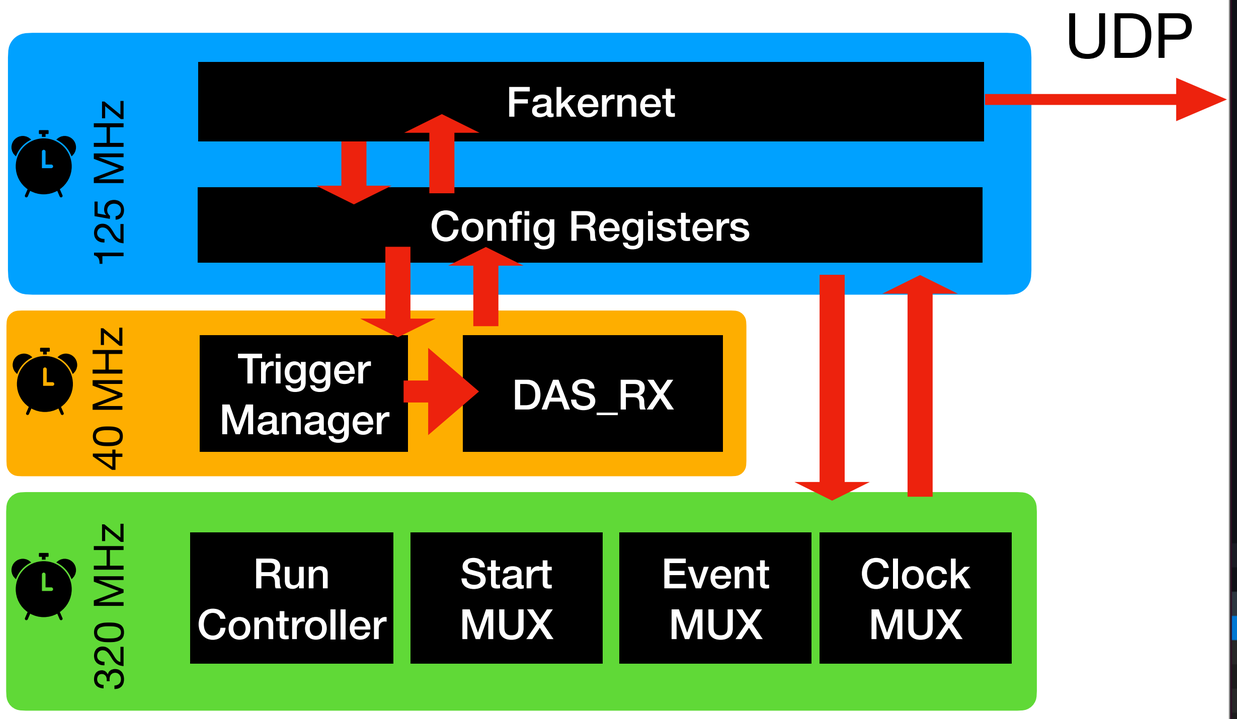
Datapath



10

Firmware description

Slow control



UDP

[1]

```
Board Detail: 201

Name        201
Type        samidare
ASIC        unknown
FPGA        unknown
Firmware    unknown
Connected   yes
Fresh       yes
Powered     yes
Acquiring   no
Run Armed   yes
Run Active  no
RX Ready    yes
Primed      no
Cfg Fault   no
Run Status  0x00000029
Cal Ready   no
Cal Failed  yes
Cal State   lock
Cal Status  0x0000000f
Clock Done  -
Lane Done   -
Failed      []
RX Locked   0x0
RX SyncErr  0x0
FIFO Empty  0xf
FIFO Full   0x0

esc Back   r Refresh   c Connect   x Disconnect   o Power on   f Power off   s Arm acquisition   t
Parameters: select a row and press Enter to edit
```

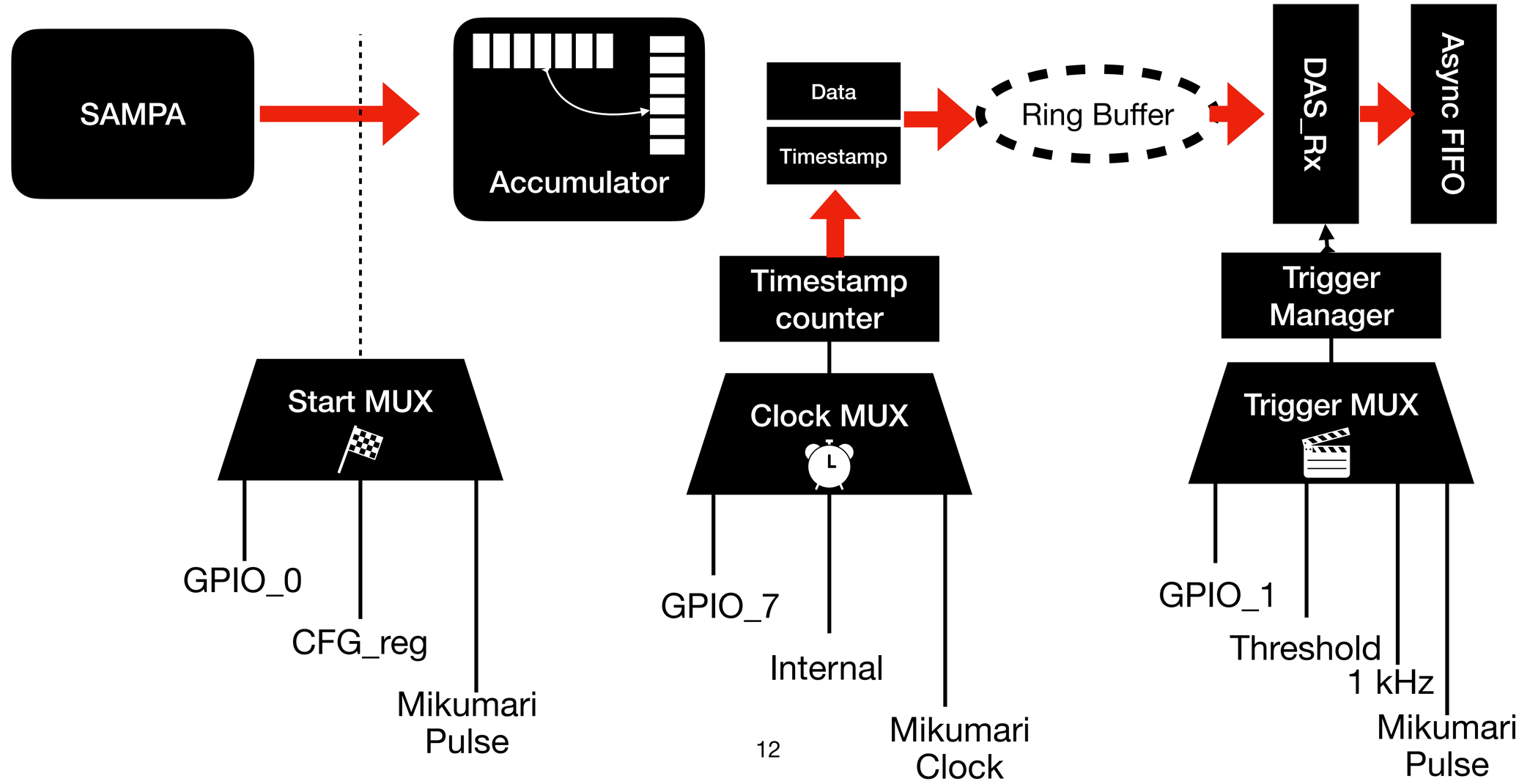
scope	parameter	current	default	options	description
global	start_source	gpio0	local	local, gpio0	Run-start source
global	event_source	gpio1	gpio1	gpio1, self, 1khz, 10khz	Event-trigger source
global	trigger_threshold	0	0		Self-trigger threshold
global	polarity	positive	negative	positive, negative	Input signal polarity
global	gain	1	1	1, 2, 3	Gain/shaping preset: 1=30
global	samples	16	16	16, 32, 64, 128	Samples from the always-i
global	pretrigger	0	0	0, 4, 8, 16	Additional samples before
global	clock_source	mikumari	internal	internal, gpio, mikumari	SAMPA clock source

[1] https://claus-92.github.io/clavis

11

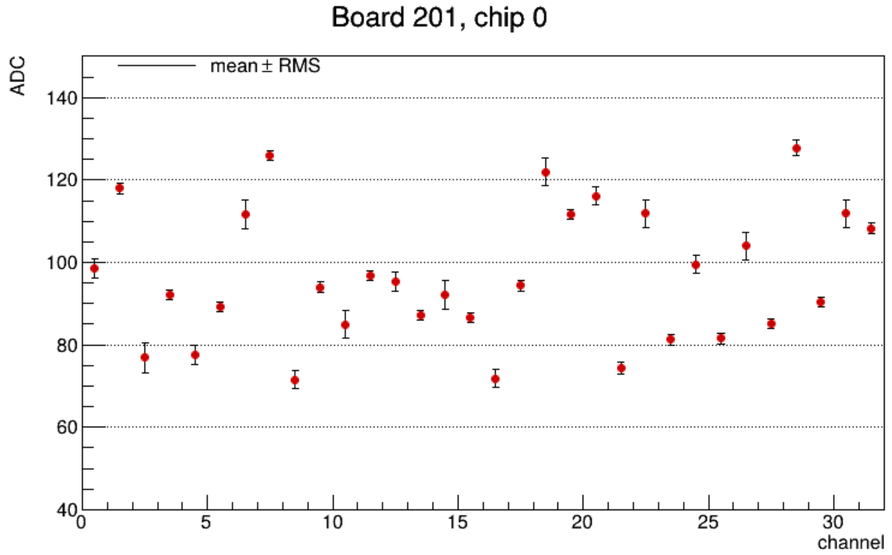
Firmware description

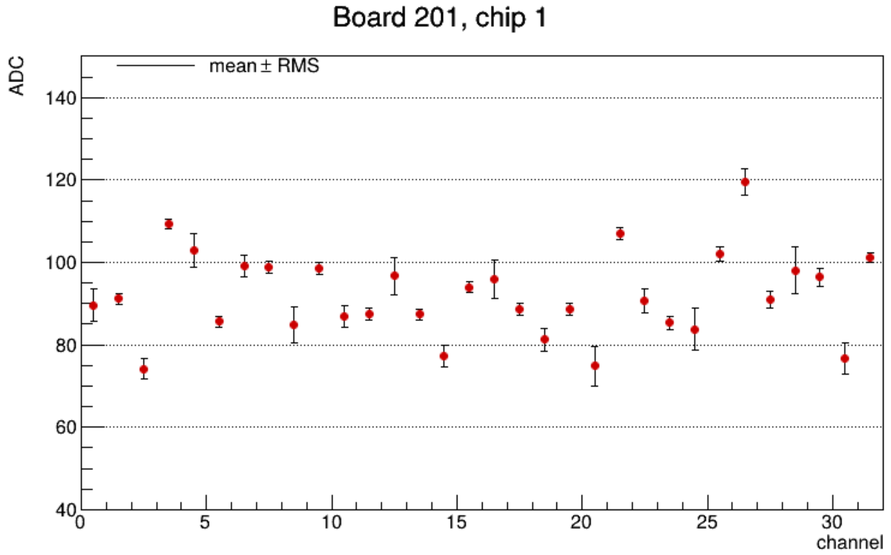
Synchronization

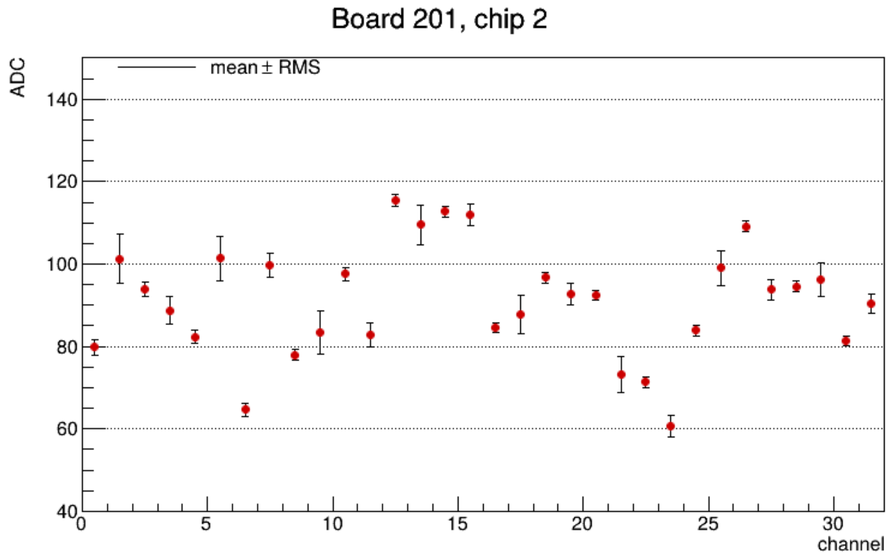


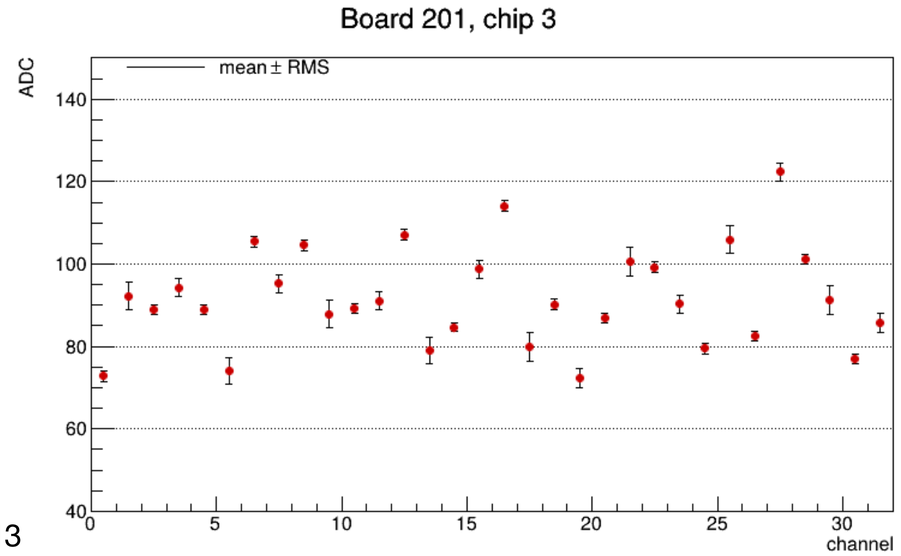
12

Pedestal and RMS









13

Trigger Rate

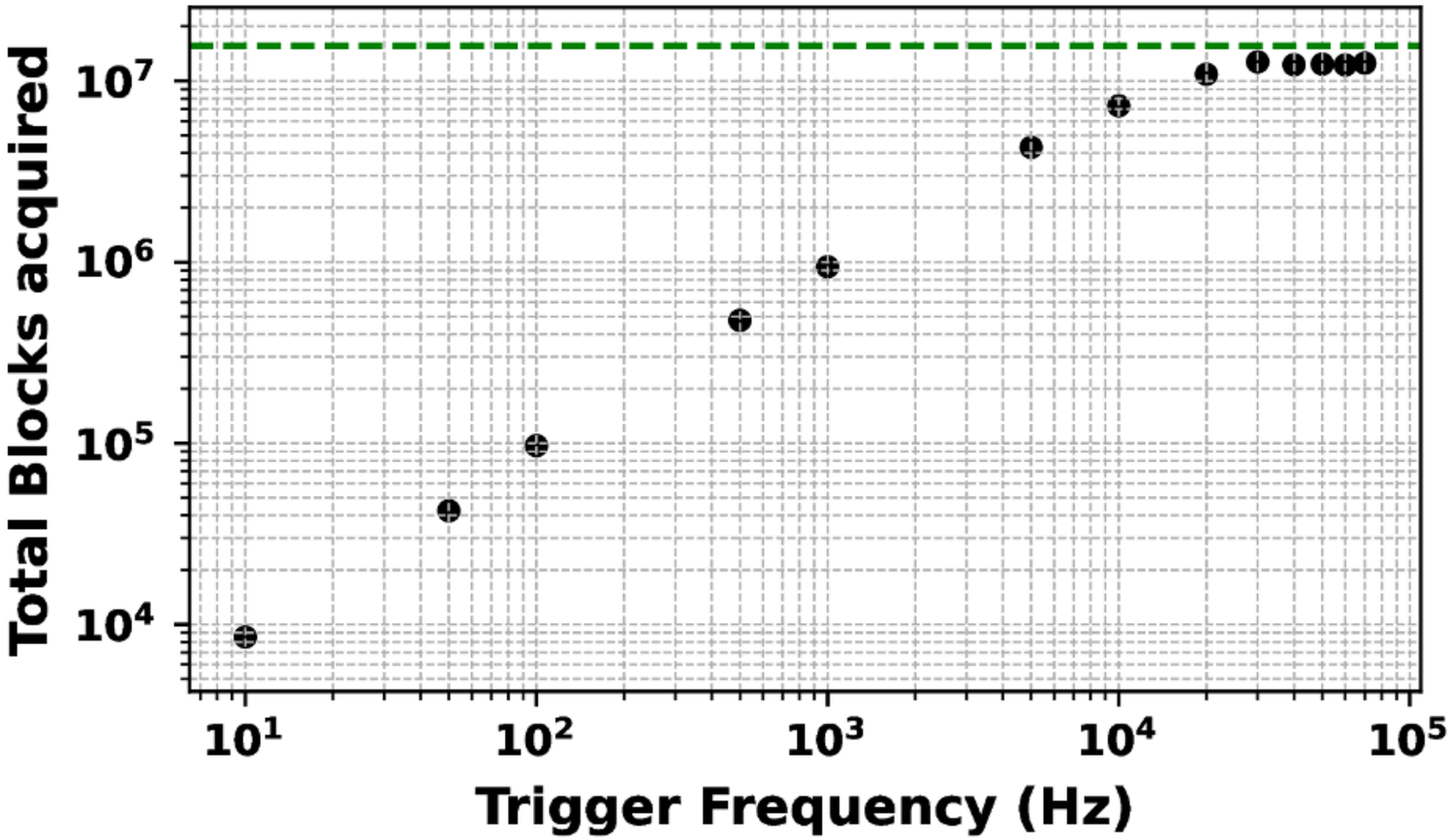
Number of event blocks acquired for 10 s acquisition as a function of trigger rate.

Event block:

32 ch x 10 bit + Metadata

Current bottleneck

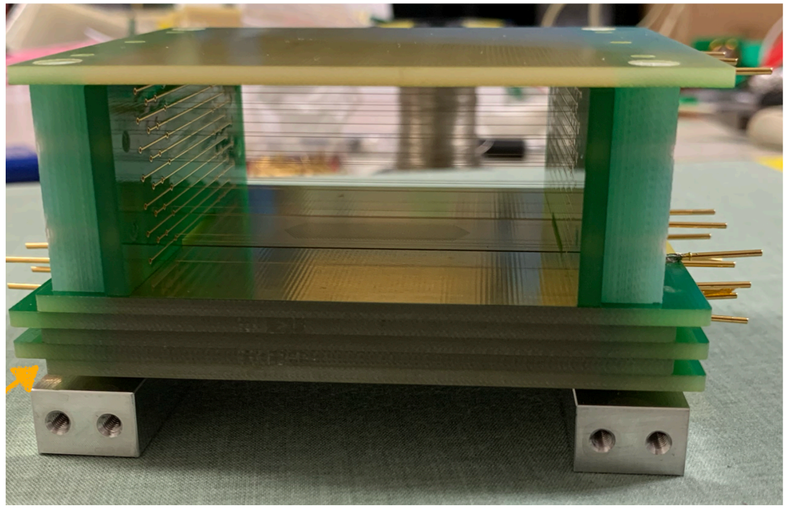
- 1 GbE Fakernet
- Zero suppression

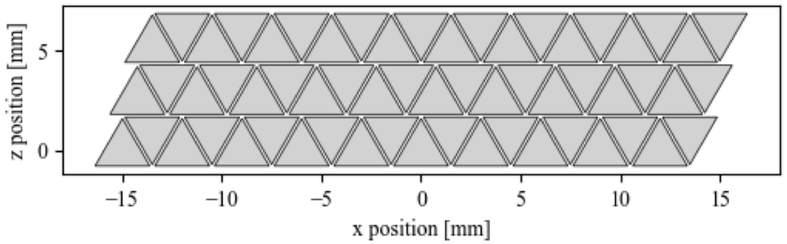


14

Single board assessment

experiment



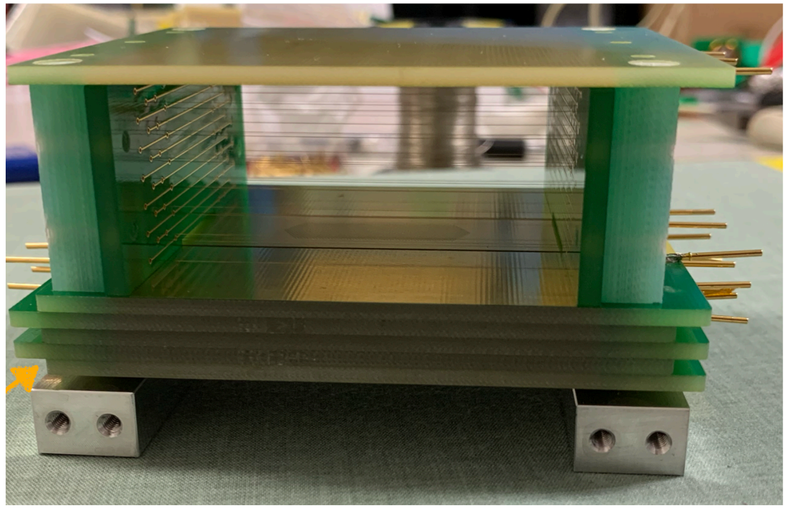


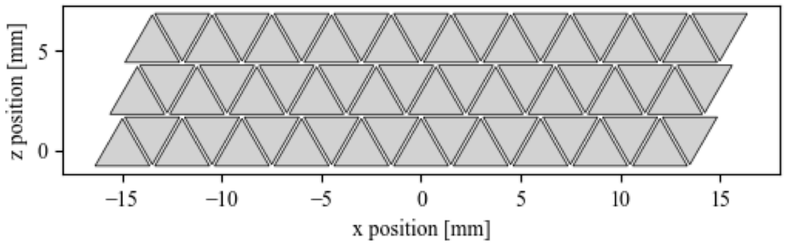
60 readout pads

Courtesy of E. Fumitaka

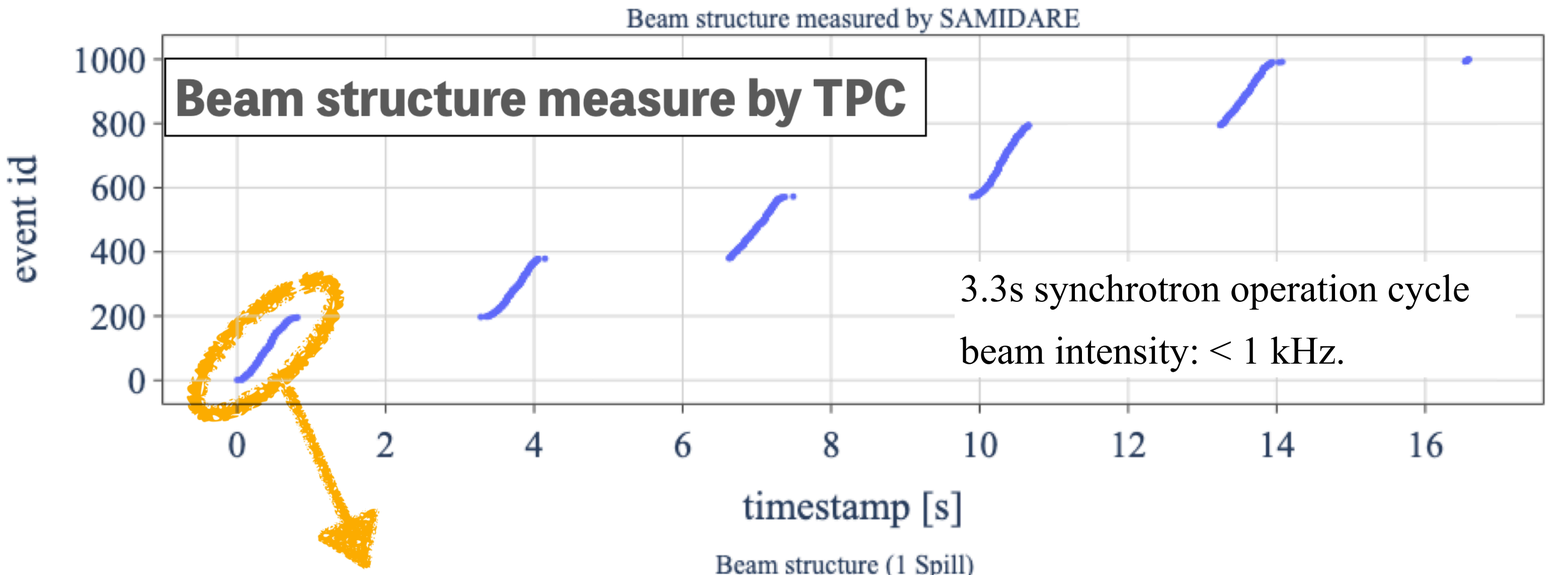
Single board assessment

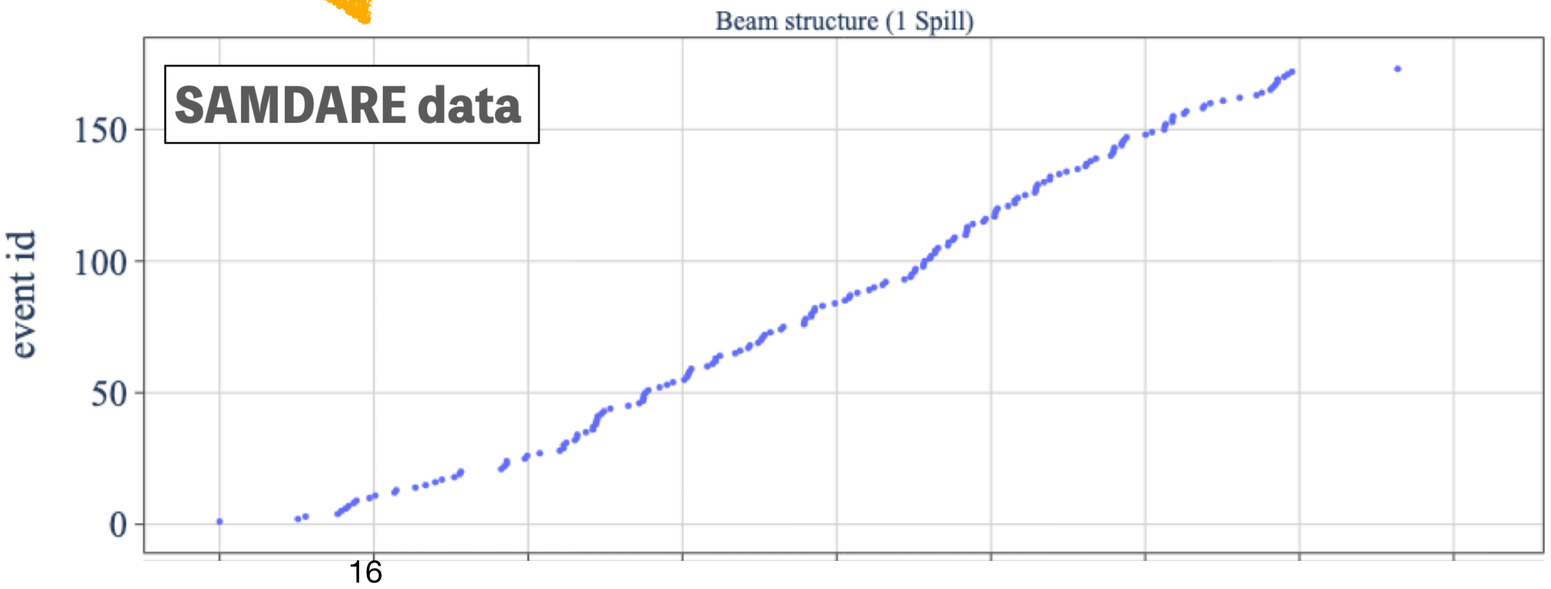
experiment





60 readout pads

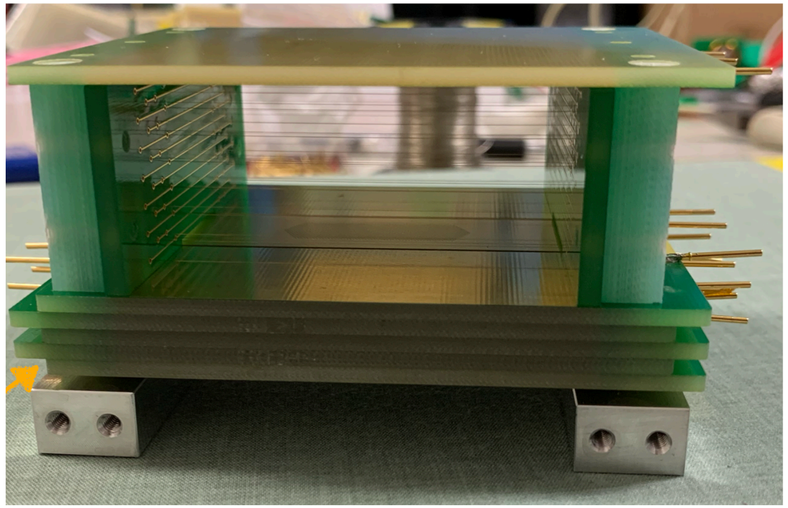


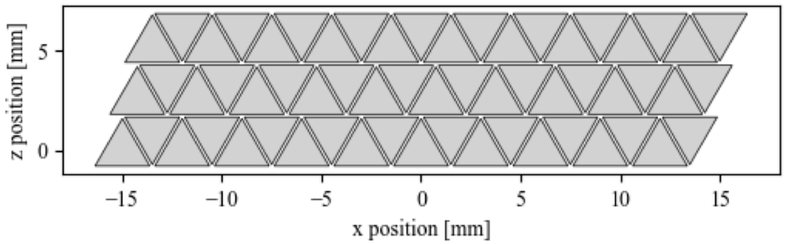


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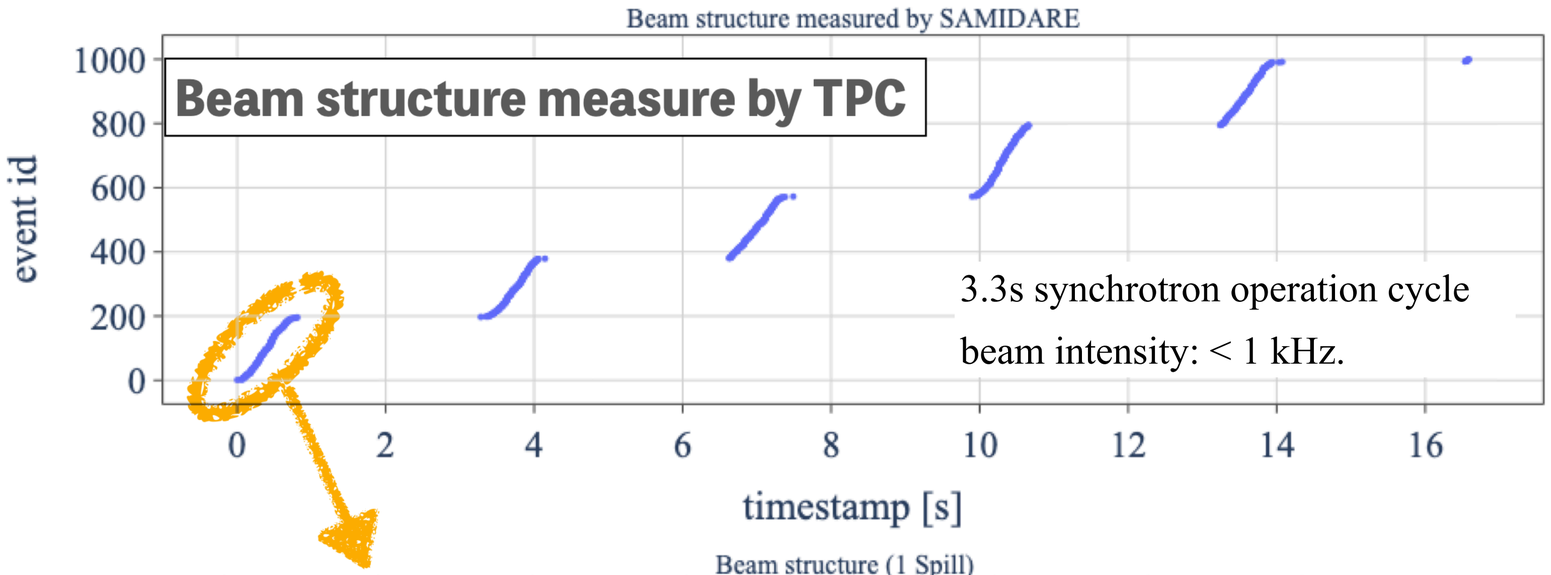
Single board assessment

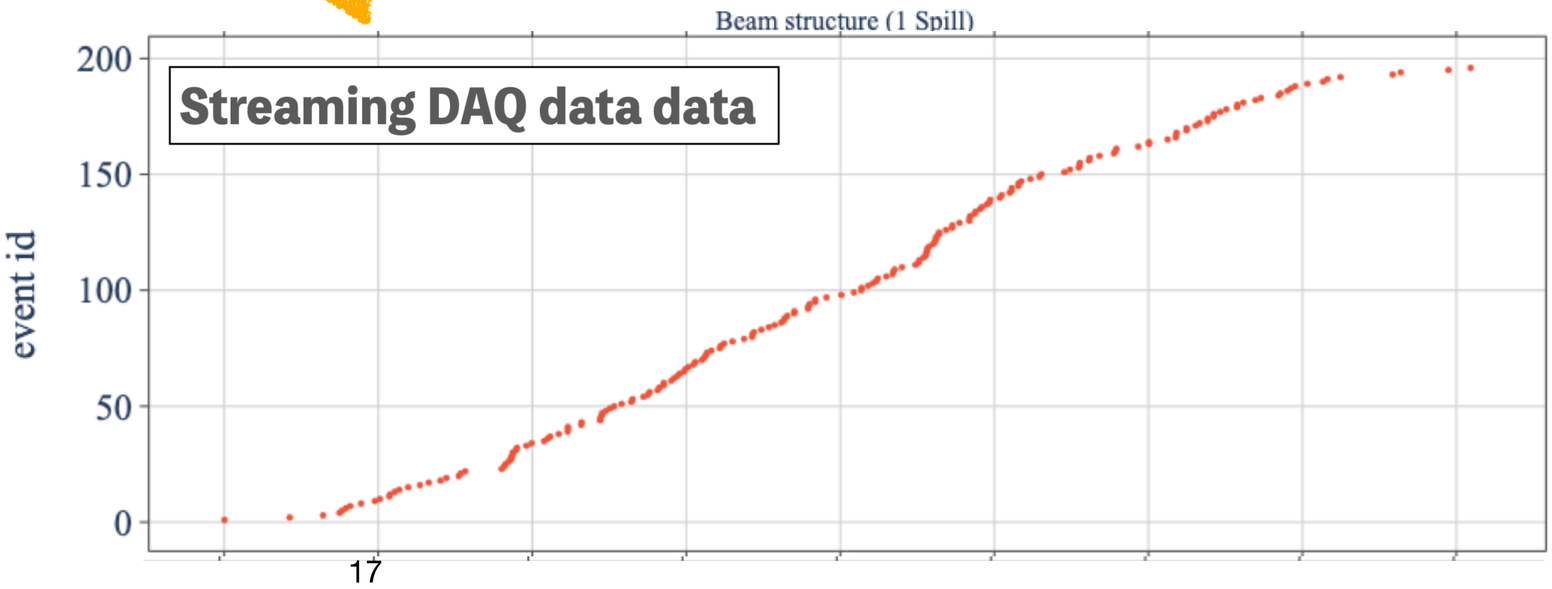
experiment





60 readout pads



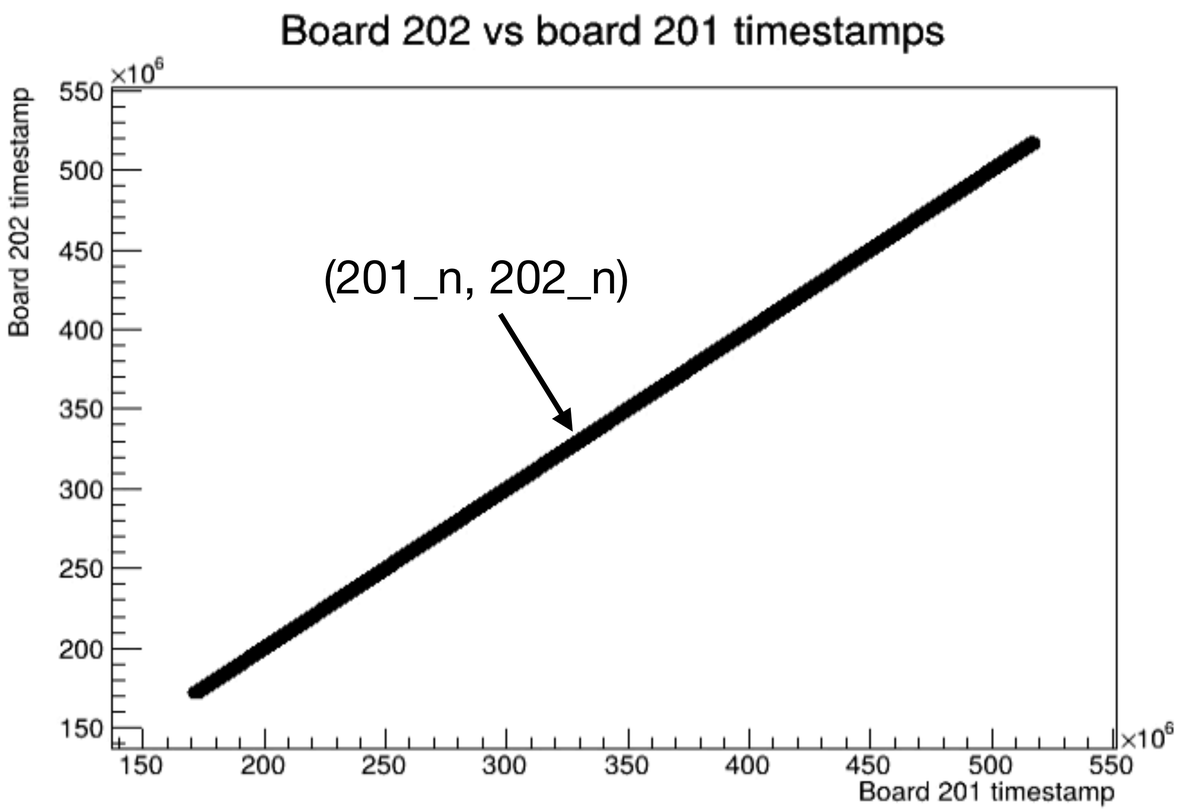


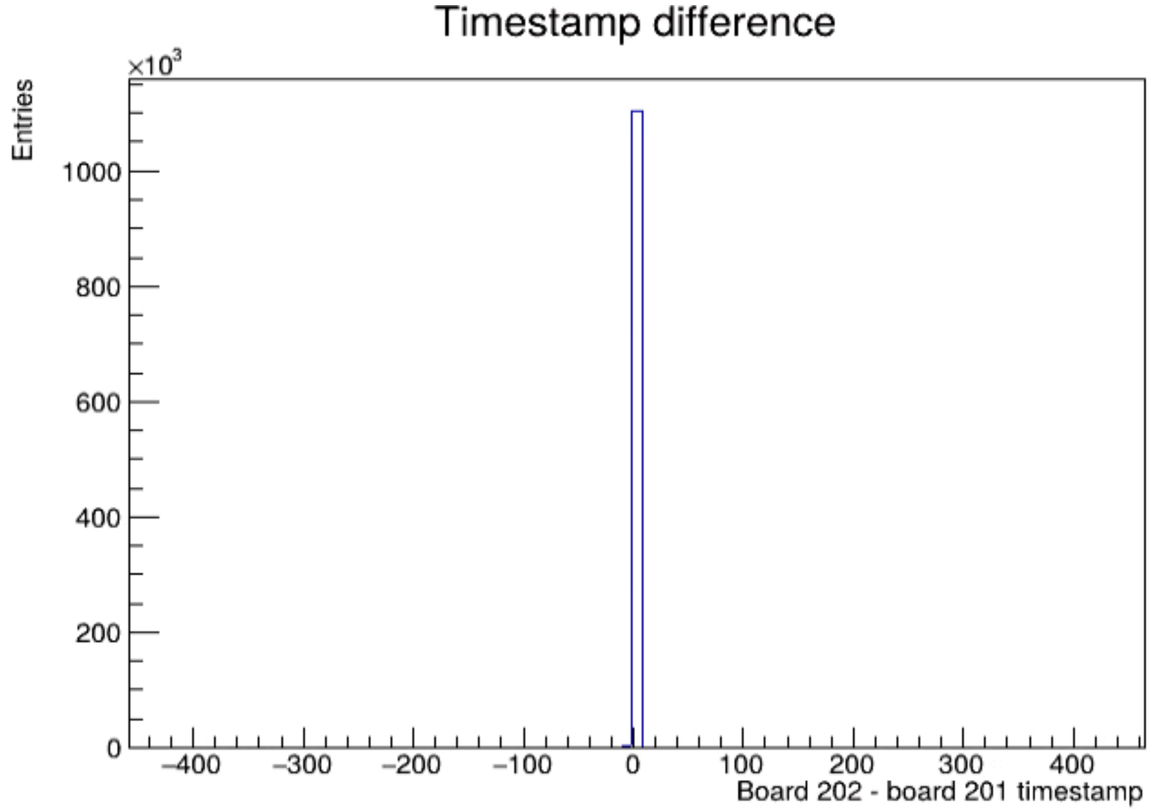
Courtesy of E. Fumitaka

17

Multiboard benchtest

Start = GPIO_0, Clock = Mikumari, Trigger= 1kHz



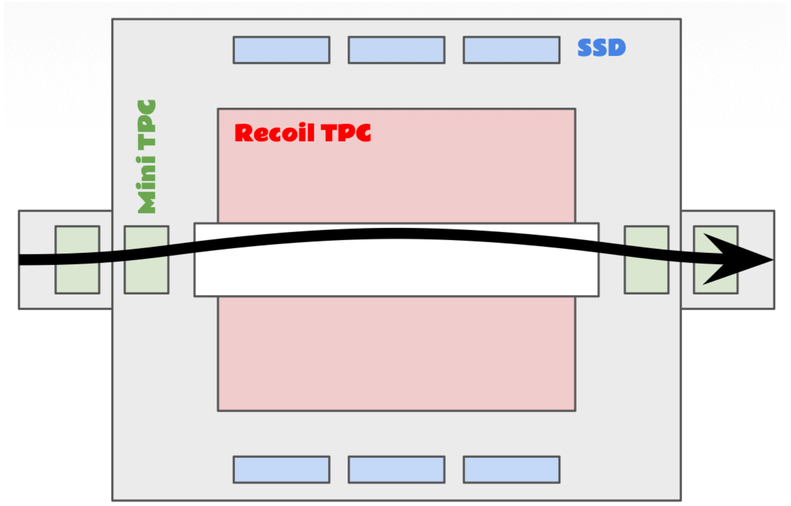


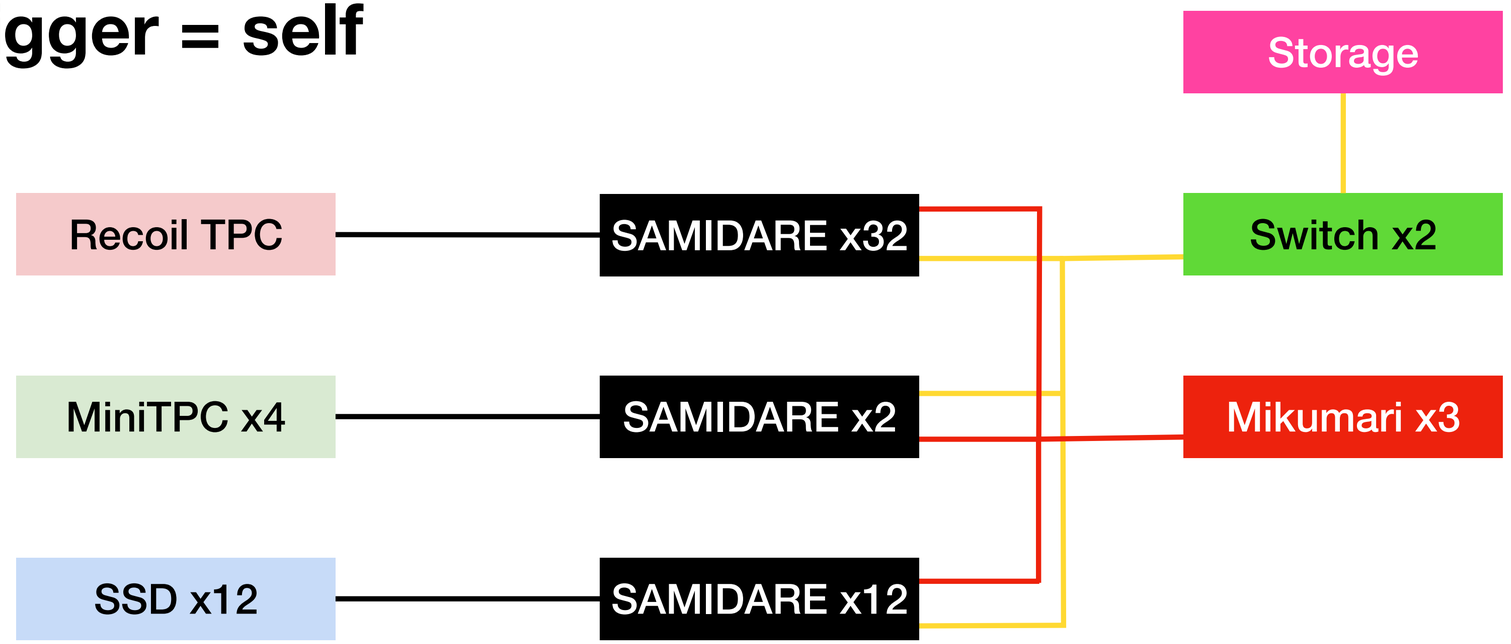
18

Multi board assessment

Fall 2026

Clock = Mikumari, Trigger = self



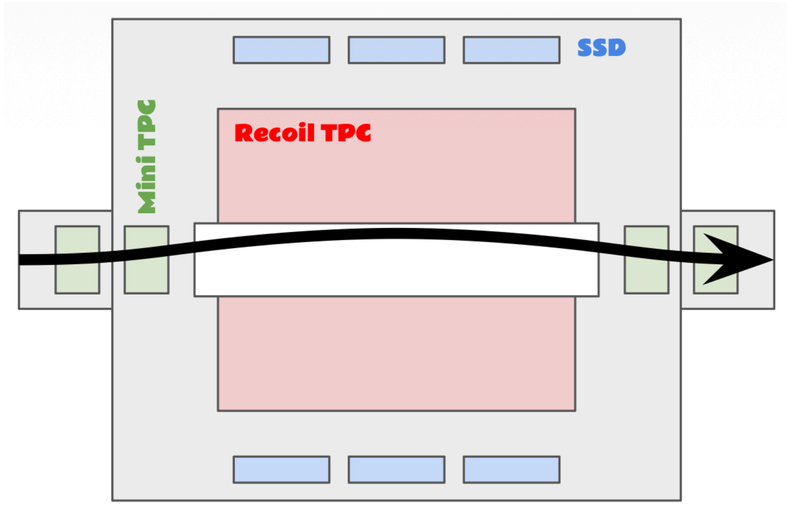


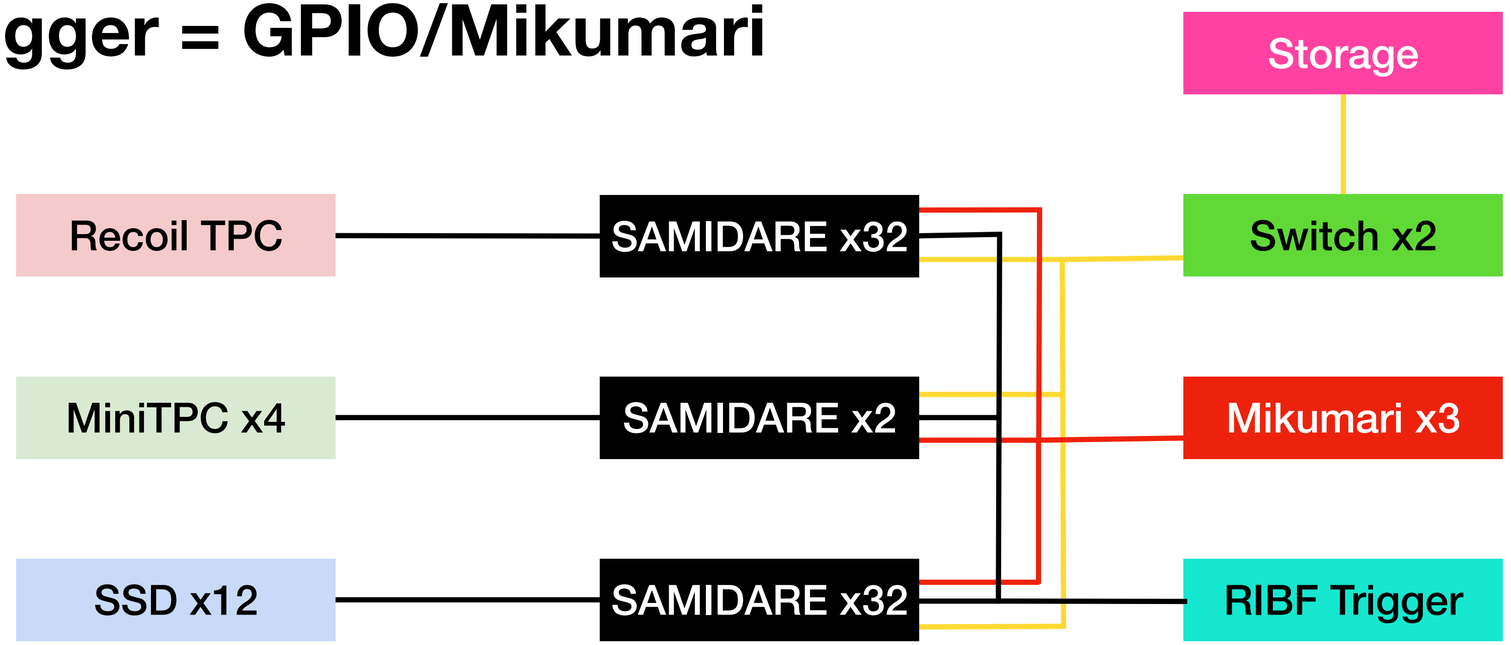
19

Multi board assessment

Fall 2026

Clock = Mikumari, Trigger = GPIO/Mikumari

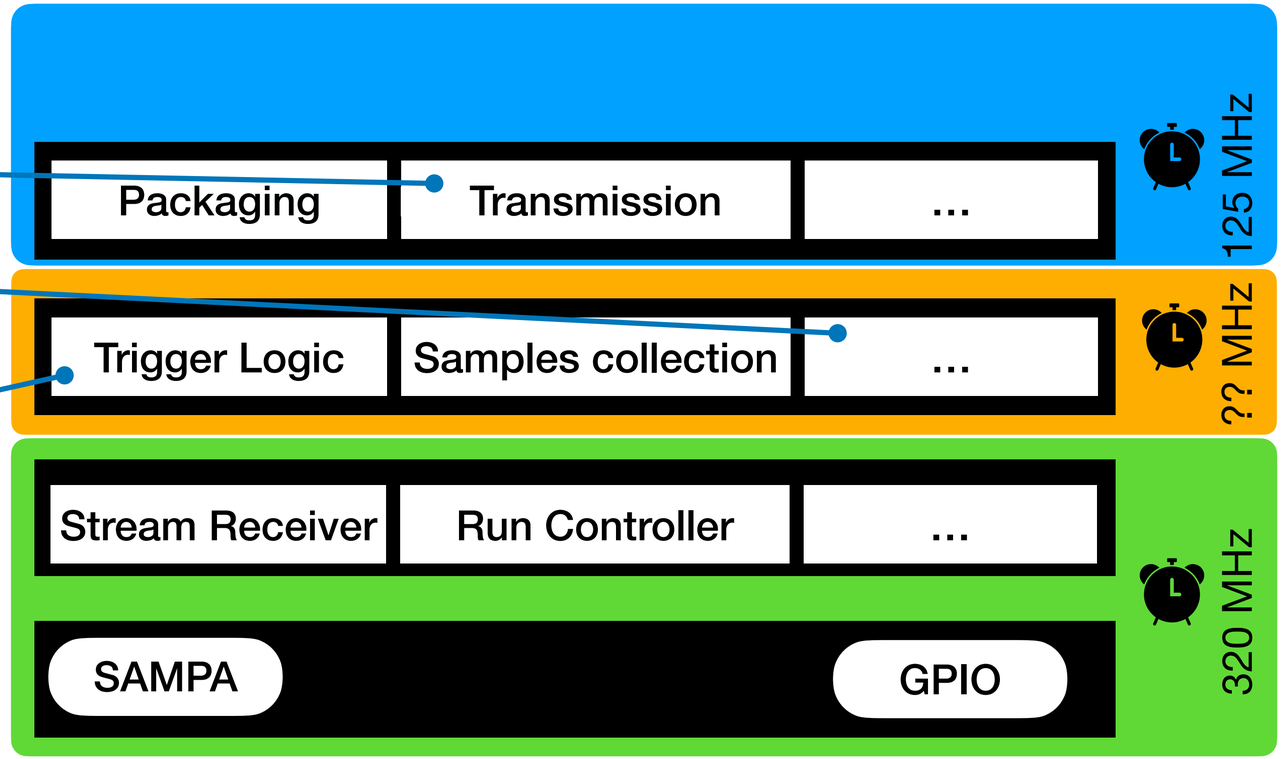




20

What’s next

- 10 Gb Data transmission
- Zero suppression
- Online beam induced background suppression



- Streaming Readout
- Specialized FW (PHA, PSA, SRO)

21

Take-home messages

SAMIDARE board

- 128 channels/board:
  4 SAMPA + FPGA + Ethernet + Mikumari

Validated

- Readout chain operation
- Bench tests
- Detector data
- Mulit-board synchronization

Next Step

- Scale up in Fall 2026
- Improve firmware
- Toward streaming readout

22