DAQ Development at RIKEN RIBF and DAQ Collaboration in Japan

Hidetada Baba (RIKEN)
+ SPADI Alliance

Topics

1. Japanese DAQ collaboration
   - SPADI Alliance
   - Streaming readout
     - Hardware, Software
2. FPGA-based Ethernet
   - Fakernet 1Gbps TCP/IP
   - 10Gbps UDP/IP
3. Clock timing synchronization
   - CTS Module
4. TPC readout
   - SAMPA ASIC
5. micro strip silicon readout
   - APV25-S1 ASIC
6. Realtime data processing
   - Alveo / Versal Board
7. in-house digitizer development
   - MIRA Module
8. Parallel VME readout
   - MPV system
9. FPGA-based very low cost TDC
   - FIT Module

collaborative DAQ development



- join all-Japan Nuclear Physics Research Labs.

SPADI Alliance

Signal processing and data acquisition infrastructure alliance

- Streaming DAQ, FPGA Ethernet, Clock Timing Synchronization, Front-end Electronics, DAQ User Interface, Analysis software etc.

SPADI Working Group

- WG1 : Front-end Electronics
  - PCB design, Firmware design, Analog, Digital etc.
- WG2 : Network and Timing Synchronization
  - WhiteRabbit, MIKUMARI, FPGA-based Ethernet etc.
- WG3 : DAQ Software
  - Software framework for streaming readout
- WG4 : On-line filtering
  - FPGA/GPU hardware acceleration
- WG5 : User interface
  - schema (how to describe DAQ system), slow control
- WG6 : Computing farm
  - Network, Server, Storage
- WG7 : Packaging
  - make a package (e.g. Docker image), manual

Some expert members
+ beginner Researcher
+ beginner PostDoc
+ beginner Student

in total, more than 130 members
(from almost all Japanese Nuclear physics labs)

Collaboration
FRIB, BNL, JLab
particle physics in Japan
new collaboration is welcome

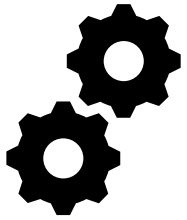
Development scheme

Multiple organizations collaborate without barriers

Sharing Challenges
Finding common issues



Define Tasks



Board design,
Firmware,
Software,
Discussion etc.

Organize Team (Task Force)



Leader (Management + Documentation)

Adviser (Expert)

work together

Beginners (Development)
student, postdoc, researcher

Development and Implementation
few months – few years



Share outputs

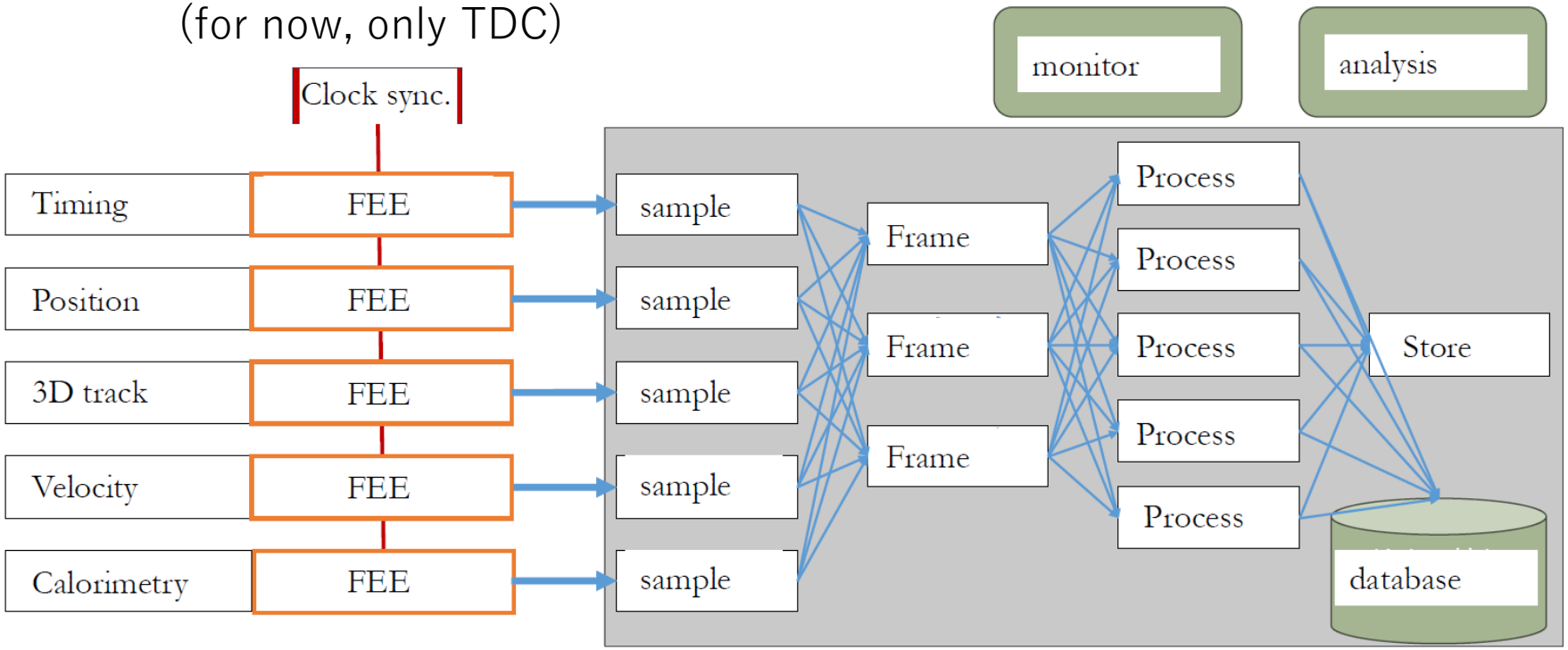
GitHub

open source or closed within SPADI
https://github.com/spadi-alliance/

Streaming Readout (no hardware trigger for readout)

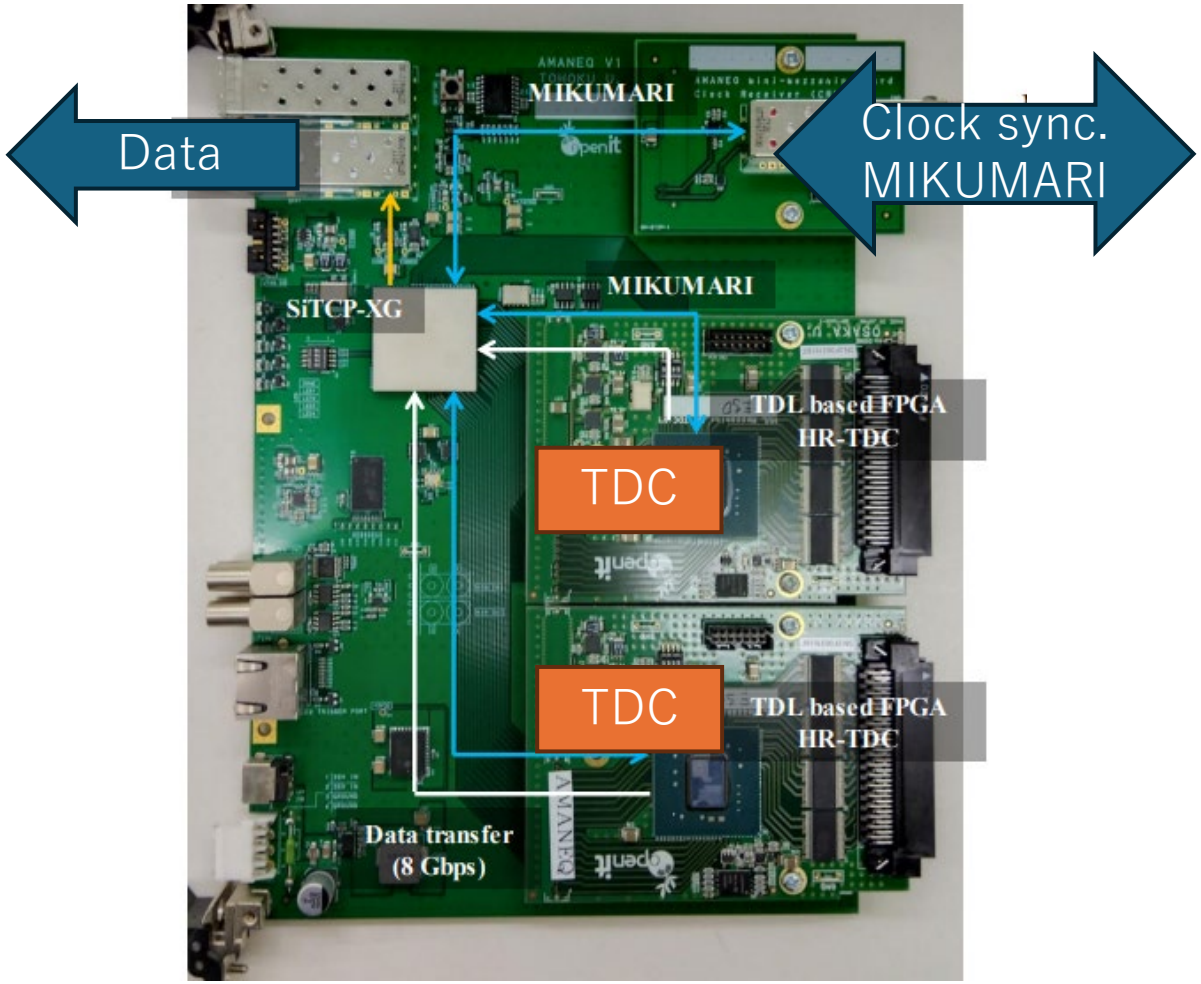
Self trigger
Timing = hit v.s. clock
(for now, only TDC)

Computing farm
online **software filter** (e.g. coincidence)



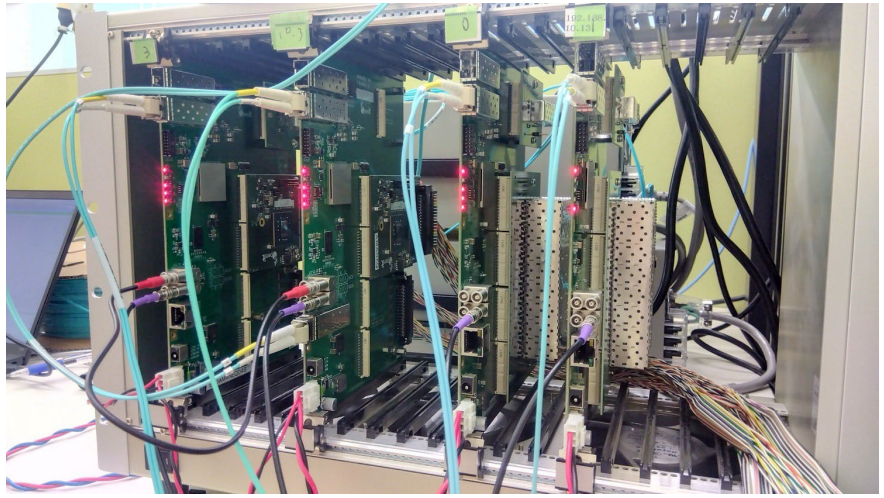
all data are sent to computing farm

Streaming readout Hardware



64 channel TDC
Low resolution : 1ns LSB or
High resolution : ~30ps(σ) TDC
MIKUMARI link (Clock synchronization)
resolution ~30ps(σ)

10Gbps FPGA-Ethernet (TCP/IP)
(commercial firmware)



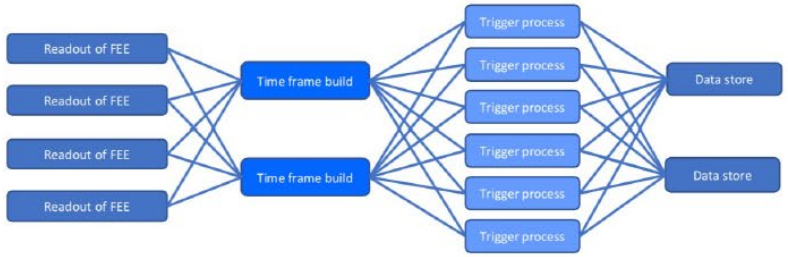
Streaming readout Software

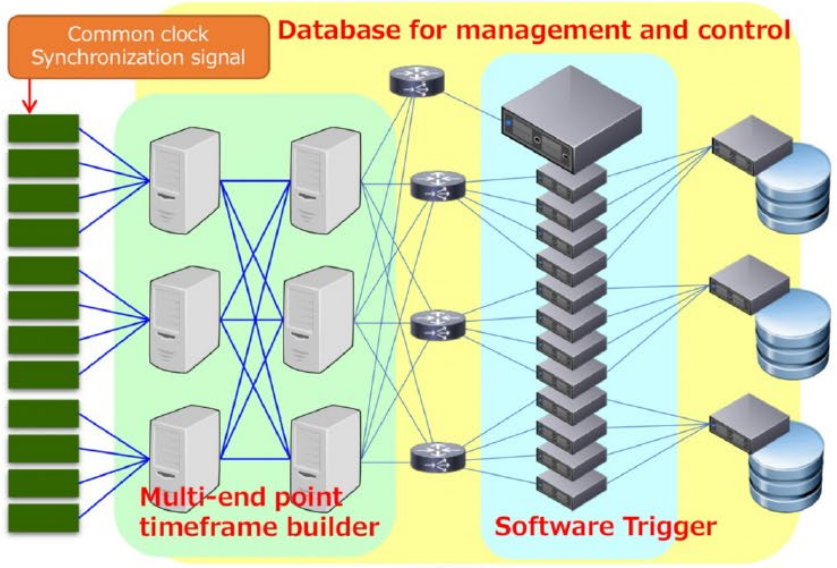
NestDAQ

https://github.com/spadi-alliance/nestdaq

DAQ framework for streaming readout

- **SPADI-Alliance has been developing the streaming DAQ framework.**
- **NestDAQ (network-based streaming DAQ)**
  - **overall management of dataflow and control**
  - **FairMQ**
    - **ZeroMQ as process communications**
      - One to many, many to one communication
      - Message queue works as a data buffer.
  - **Redis (key-value based DB)**
    - Memory-oriented and fast response
    - Key-space notification
    - Pub/Sub →It can be used for control.





Fakernet 1Gbps TCP/IP

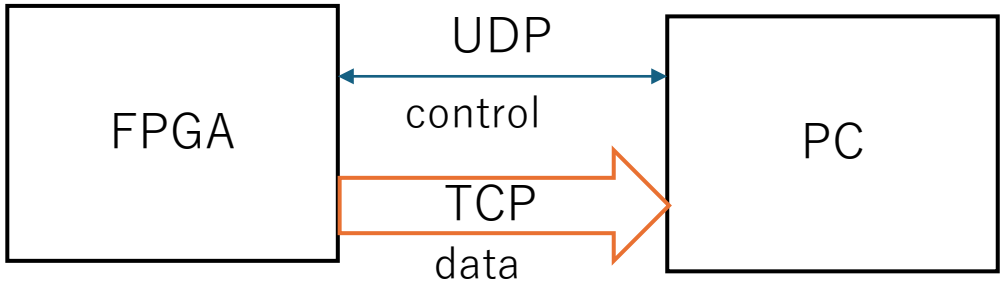
- Fakernet (open source)
  - TCP/IP protocol stack by VHDL
    - work on FPGA w/o CPU
  - developed by Hakan (Chalmers)
- our work is
  - implement on several FPGA boards
  - https://github.com/spadi-alliance/fakernet

Location

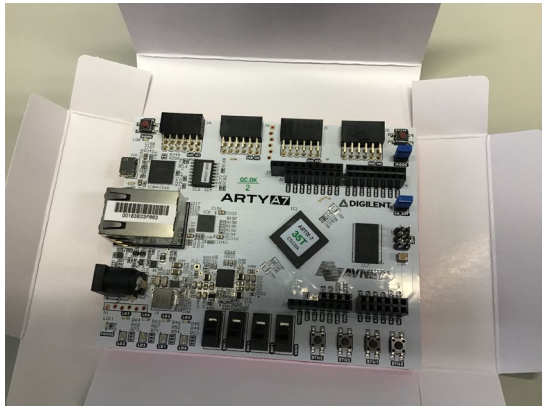
http://fy.chalmers.se/~f96hajo/fakernet/fakernet-0.9.8.tar.gz

Contact

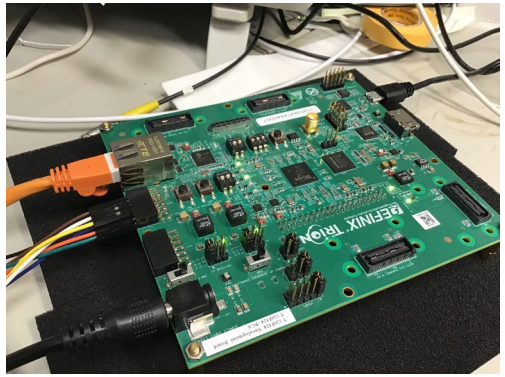
Håkan T. Johansson (f96hajo@chalmers.se)



AMD Arty Board
Artix-7



Efinix Trion T120



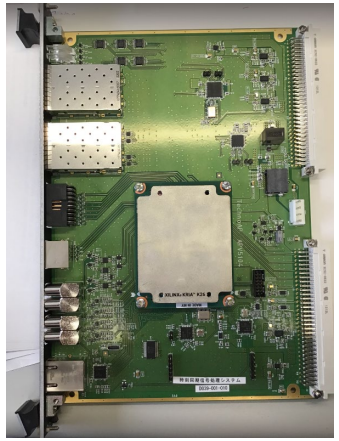
AMD
Vertex Ultrascale



AMD
Artix Ultrascale+

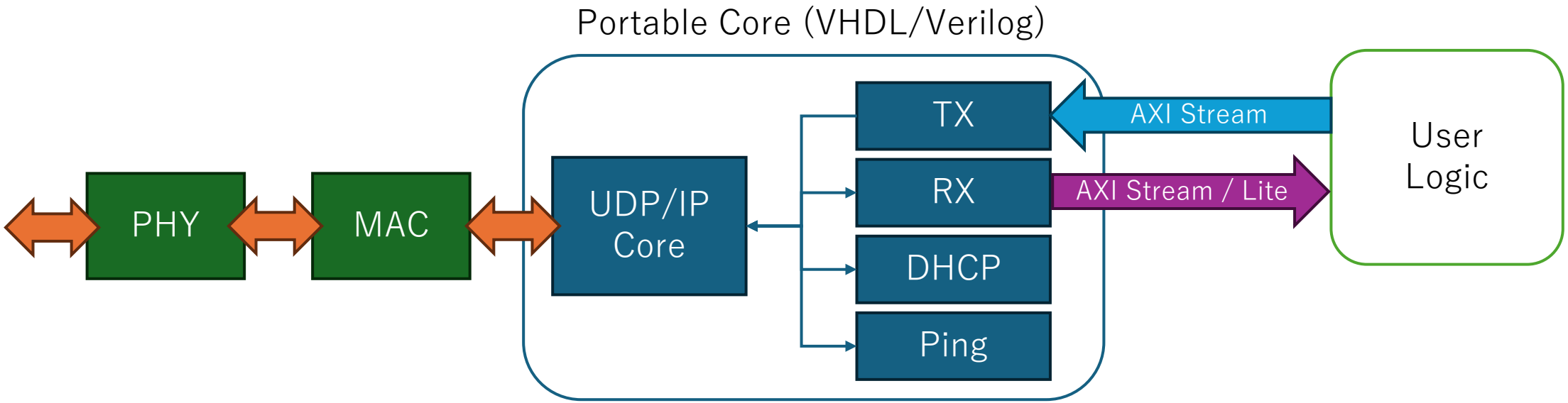


AMD **KRIA**



Portable 10G UDP/IP Core

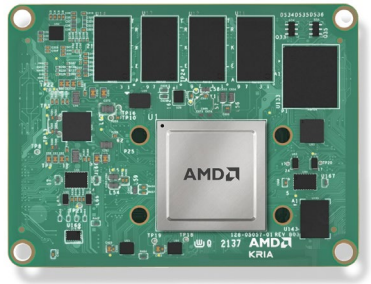
- Based on UDP/IP core from IDROGEN project in CERN
  - https://indico.fnal.gov/event/18454/contributions/47488/attachments/29593/36473/GUIYAN-DROGEN-2018.pdf
- Portable (easy-to-use) 10G UDP/IP Core
  - add the interface to User logic through AXI-bus
  - UDP/IP Core, DHCP, Ping are from IDROGEN project
- Development has just begun



Clock Timing Synchronization

- Motivation
  - **interface several different clocking system**
  - WhiteRabbit (CERN, GSI..) , MIKUMARI (SPADI, KEK), Dogma (GSI), etc.
  - WhiteRabbit implementation
    - talk by Ginie today 14:30--
    - **FRIB-RIKEN R&D: CTS Board for Clock Translation**
- CTS board
  - KRIA = SoM
    - FPGA(w/ Arm CPU core)
      - 4 GTH 12.5 Gb/s Transceiver
      - 116 I/O (High speed) + 69 I/O (Low speed)
    - DDR memory
    - Flash memory
  - On board components
    - 4 different PLLs
    - SFP+ for Gigabit transceiver
    - SFP+ for High speed I/O
    - 4 NIM Output, 4 NIM Input
    - 12 LVVS I/O

AMD KRIA $325





TPC readout

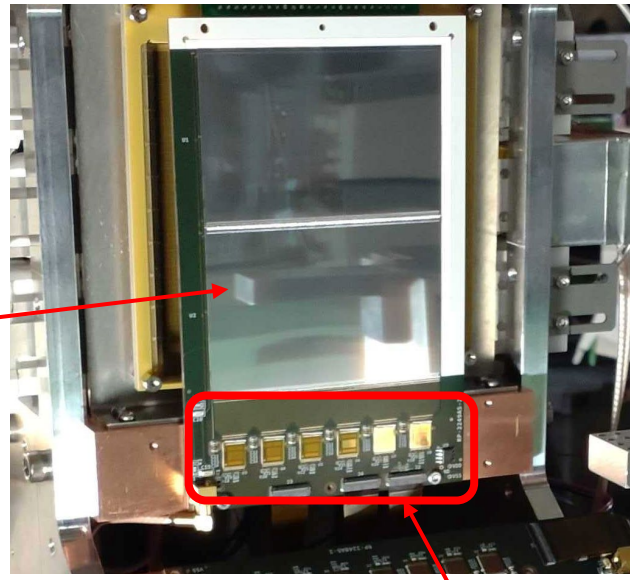
- SAMIDARE board
  - SAMPA ASIC x 4
    - 128ch input
  - for now
    - Ethernet (1Gbps Fakernet)
    - simple internal /external trigger
  - future
    - 10G UDP
    - MIKUMARI link + streaming readout
- related talks
  - Caludio, yesterday 10:30—
    - Active Target TPC Development for Alpha Scattering at RIBF
  - Endo, today 14:00—
    - Commissioning Test of the SAMIDARE Board Using the Mini TPC Towards the Upgrade for CNS Active Target



micro strip silicon readout

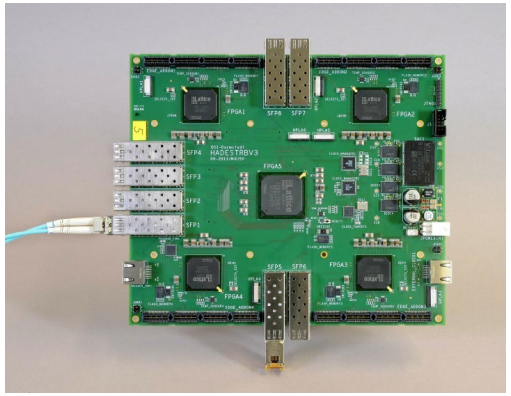
- APV25-S1 ASIC (256ch / chip)
  - many channel readout ASIC by CERN
  - for position + dE
  - If there is a good successor ASIC, please let me know!

100um pitch
100um thickness
silicon strip sensor



APV25-S1

Readout
ADCM (TU Munich) + TRB3 (GSI)



Realtime data processing

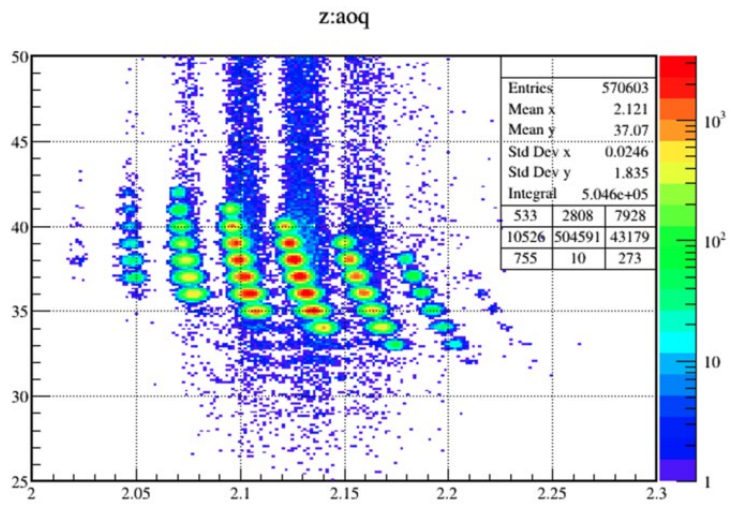
- poster (tomorrow)
  - Yuto Ichinohe (Poster)
    - **Streaming data processing using Alveo/Versal data-center accelerator cards**

Xilinx Alveo
FPGA card



Xilinx Versal
FPGA+AI



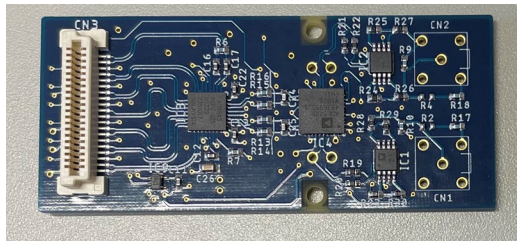


Particle identification analysis case,
throughput 40M event/sec

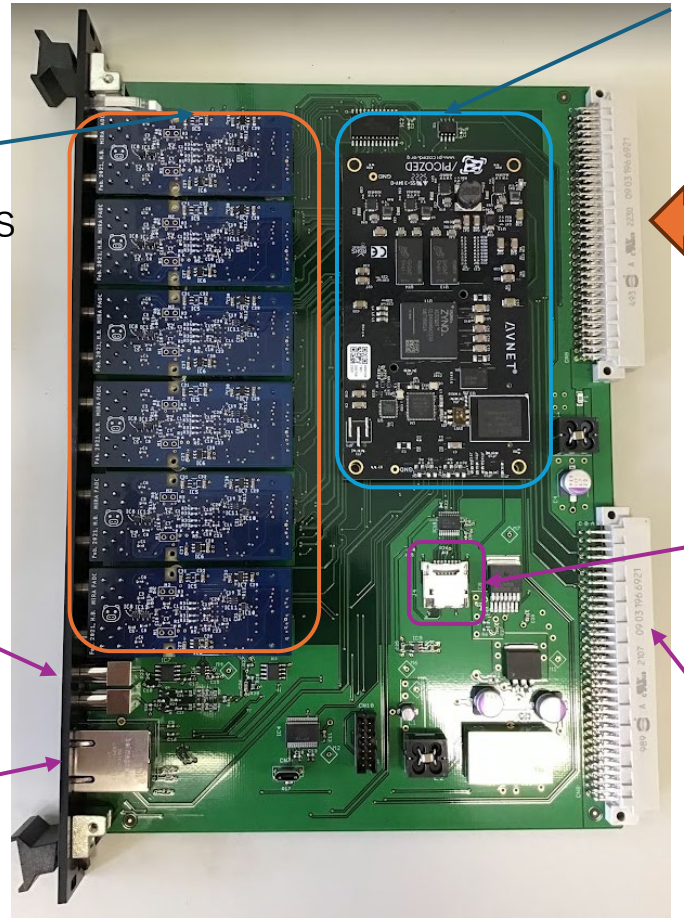
C++ code -> FPGA circuit

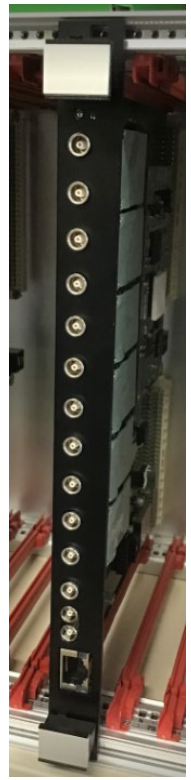
in-house digitizer development

today 15:00– talk by Kitamura
In-House Development and Implementation of Waveform Digitizers at RIBF



AD9645
2ch, 14bit, 125MHz



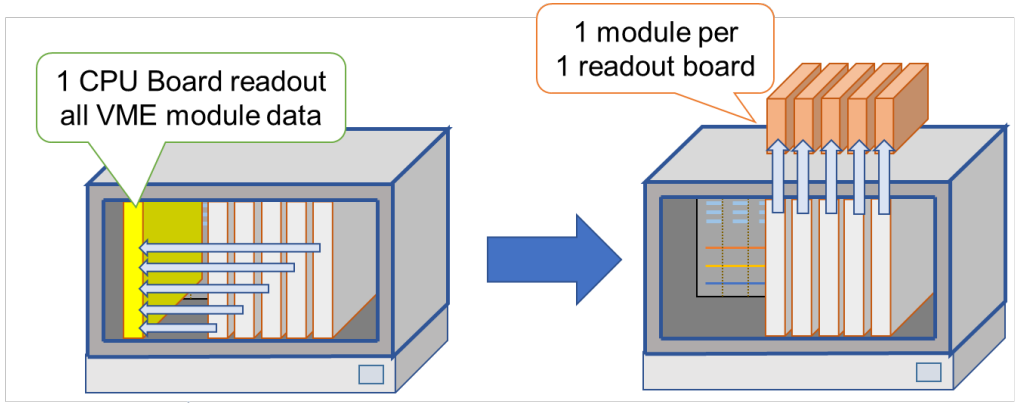


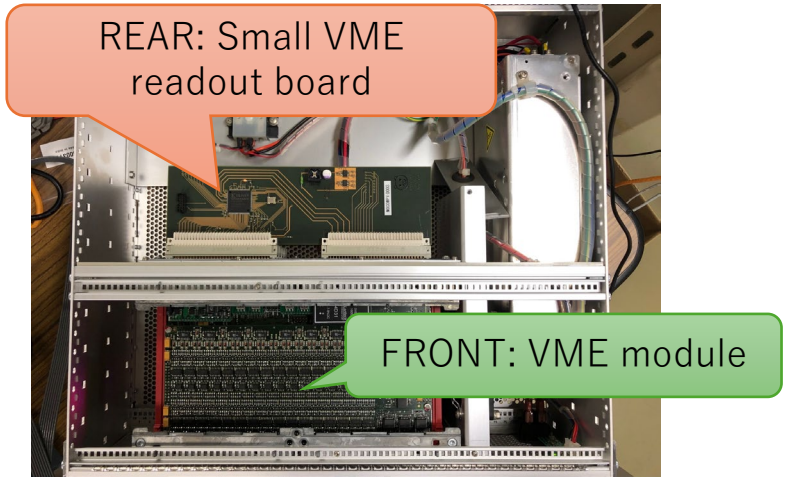
H.Baba et al., IEEE TNS 68 (2021) 1841

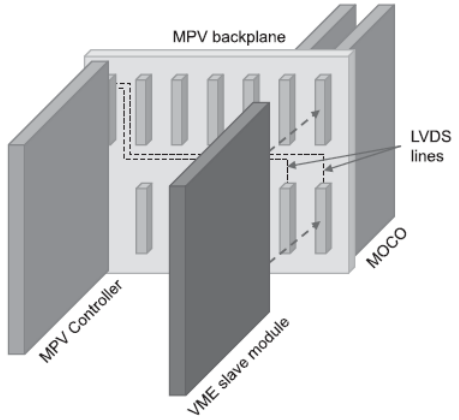
MPV : Parallel VME readout system

Compatible with standard VME module









Readout
～ 100us
(OS Latency ～20us)

Parallelize!!

Readout
<< 20us
(no OS latency)

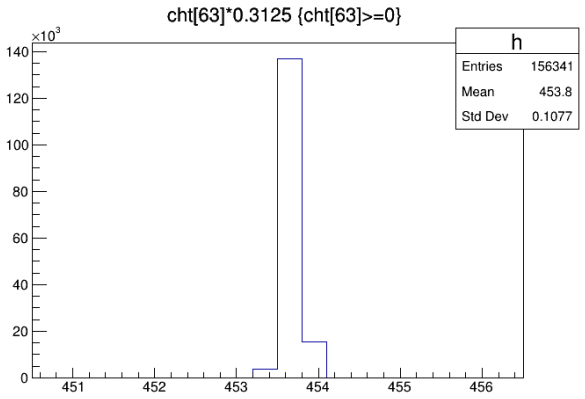
Crate Parallel

Module Parallel

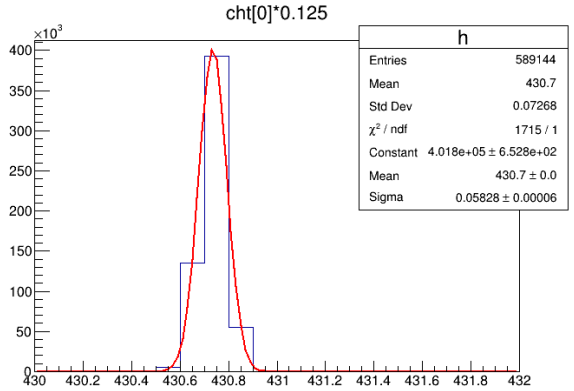
stably working in RIBF, 25kHz trigger rate is acceptable even with standard VME modules
support modules (CAEN V7XX/V1X90, Mesytec MADC/QDC/TDC/DPP, SIS 3820 etc.)

FPGA-based Very low-cost TDC

- multi-phase clock FPGA TDC
- Two firmware versions
- 64ch, 312.5ps leading/trailing edge
- 64ch, 125ps leading edge only

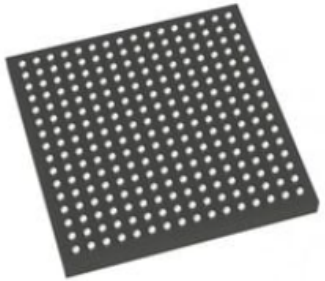


LSB 312.5ps
(FWHM 253ps)



LSB 125ps
(FWHM 137ps)

AMD Artix 7



XC7A50T-2FTG256I

DigiKey Part Number	122-1918-ND
Manufacturer	AMD
Manufacturer Product Number	XC7A50T-2FTG256I
Description	IC FPGA 170 I/O 256FTBGA
Manufacturer Standard Lead Time	16 Weeks

QUANTITY	UNIT PRICE
1	$91.21000

FIT Module



64 channel board, cost = $270

$4.2 per channel

Summary

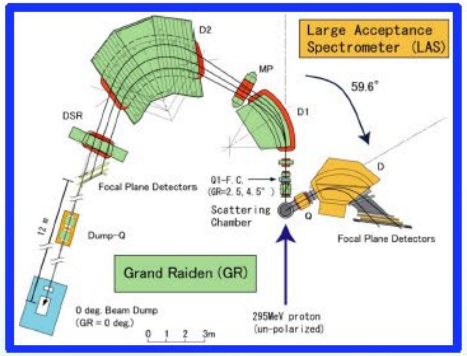
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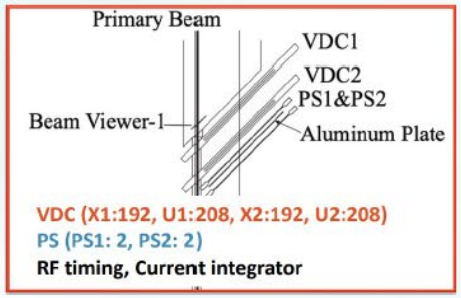
- **New collaboration is welcome !!**

backup slides

Streaming readout

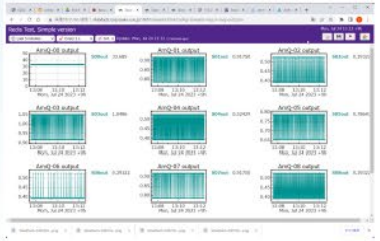
Example of Topology (tested 2023.7 at RCNP)



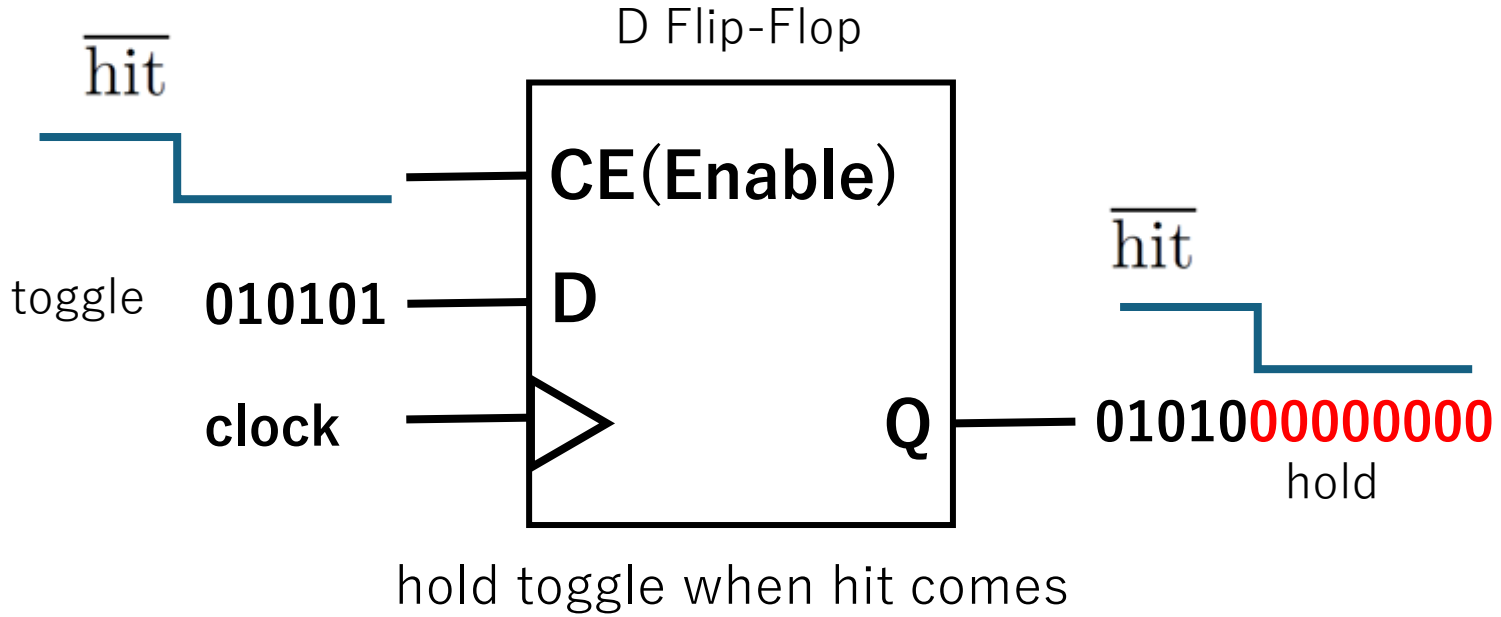






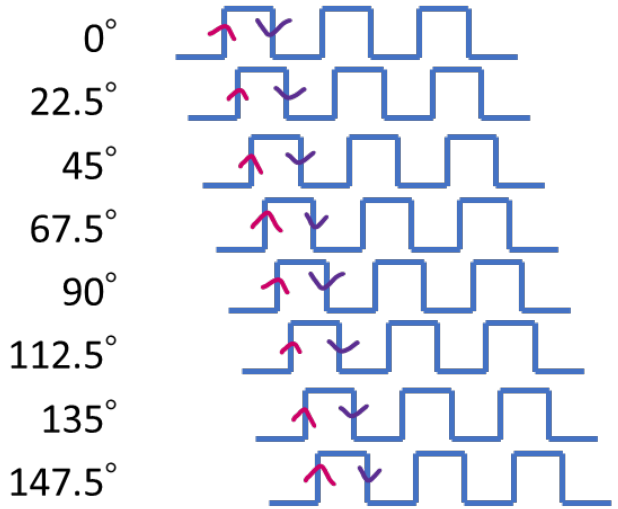


Principle

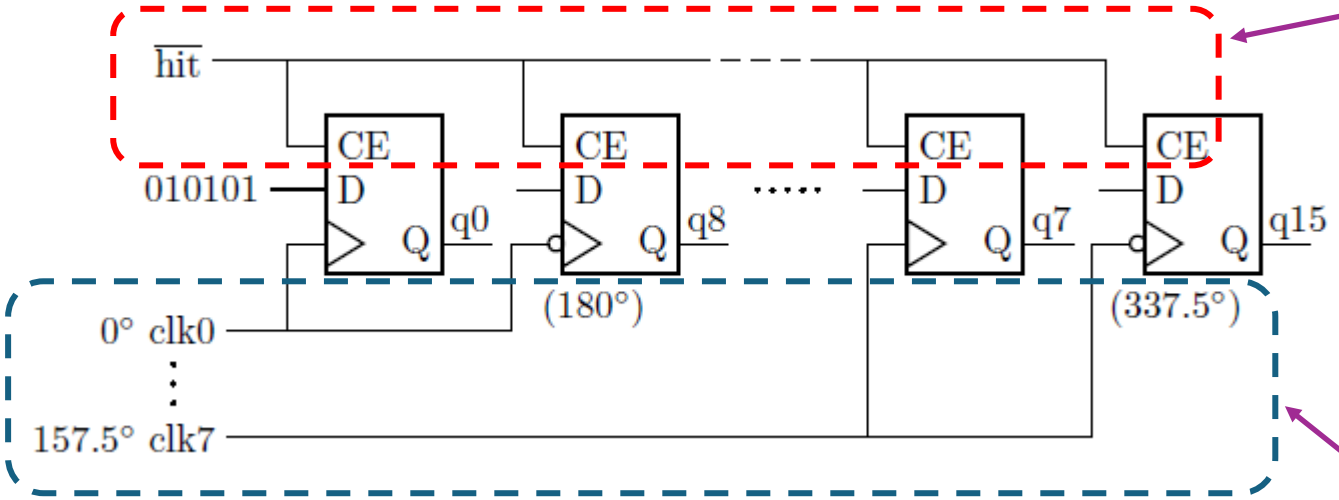


hold toggle when hit comes

16 different clock phases
500MHz : 2ns / 16 = 125ps
200MHz : 5ns / 16 = 312.5ps

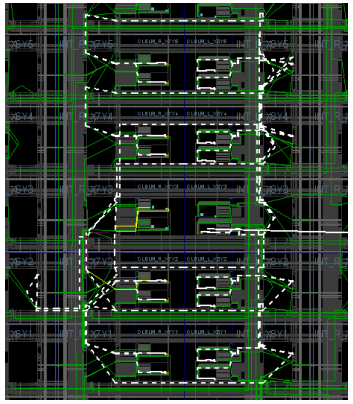


key point = wiring in FPGA



fan-out hit signal to 16 flip-flop components, the skew of this fan-out is crucial.
Do manual wiring to minimize the skew using AMD Vivado tool.
now +/- 20ps skew is achieved.
(without manual wiring, skew will be > 400ps)

manual wiring in FPGA



for clock distribution, use clock lines (very small skew) in FPGA, but, only 12 lines are available in Artix-7

pattern will be 0000111111111111
1111000000000000 → both cases, value = “4”